

Introduction

Powering sequencing poses a unique problem to power management. Since improper sequencing may cause damage to many types of processors, power-up sequencing of these devices is critical. Devices that may require power-up sequencing include FPGAs, ASICs and DSPs. These devices can require tracking I/O and core voltages. Requirements for power-up sequencing for specific devices may change from device and manufacturer, so it is highly recommended that sequencing requirements are reviewed for each particular device. For this example Xilinx's power-up requirements for the Spartan-II and Spartan-IIE families are used. The I/O voltage must turn on between 2ms and 50ms. Also, the slew rate of the supply voltage must not exceed 900mV/ms or rise slower than 50mV/ms. Figure 1 solves this issue, allowing for consistent and reliable power-up sequencing.

Basic I/O Voltage Control

The power-up sequencing circuit uses an RC (R3 and C3) timing network to control the slew rate of the output during turn-on. U2 compares the output of the LDO to the voltage at the RC network and adjusts the output of the regulator through the feedback voltage to match the RC charge voltage. When the voltage between R3 and C3 reaches the

LDO's regulation voltage, the output of U2 pulls low, reverse biasing D1, removing the power-up sequencing circuit from the control loop. The power-up time can be calculated as follows:

$$\left[\frac{-C3}{t} \times \ln \left(\frac{-V_{OUT}}{V_{IN}} + 1 \right) \right] - 1 = R3$$

Where t is the turn on time in seconds.

R4 and C4 provide compensation to maintain a smooth voltage during the turn-on cycle. R1 and R2 provide the output regulation voltage and can be calculated as follows:

$$R1 = R2 \left(\frac{V_{OUT}}{1.240} - 1 \right)$$

I/O and Core Sequencing

Figure 3 is an I/O and core voltage sequencing circuit. The I/O voltage is controlled by an RC network as described in the basic I/O control section. The core voltage, instead of using an RC charge voltage to control the turn-on, uses the I/O voltage ramp. U3 of the core regulator compares the output of the I/O during turn-on and matches the core voltage until regulation is reached. Figure 3 shows the I/O and core voltages during the power on cycle. Equally important is the power down cycle. The I/O voltage must never be 0.6V below the core voltage. This condition can be forward bias the substrate diode, damaging the processor. D2, a Schottky diode with a forward voltage drop of 0.4V, keeps the I/O voltage from dropping 0.6V below the core voltage during the power down cycle (Figure 5).

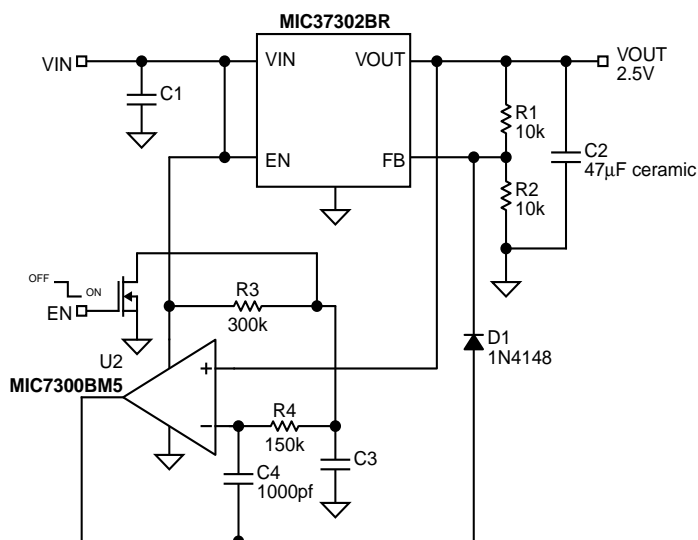


Figure 1.

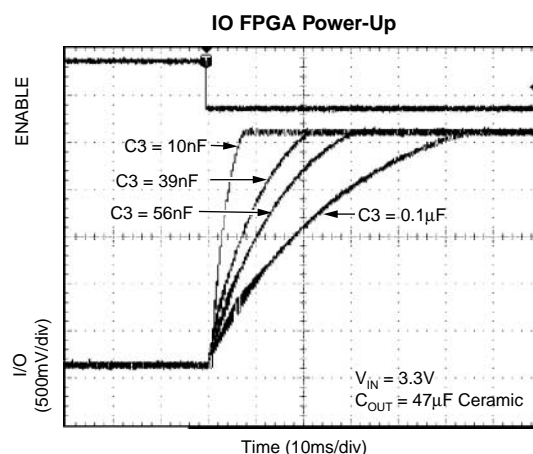


Figure 2

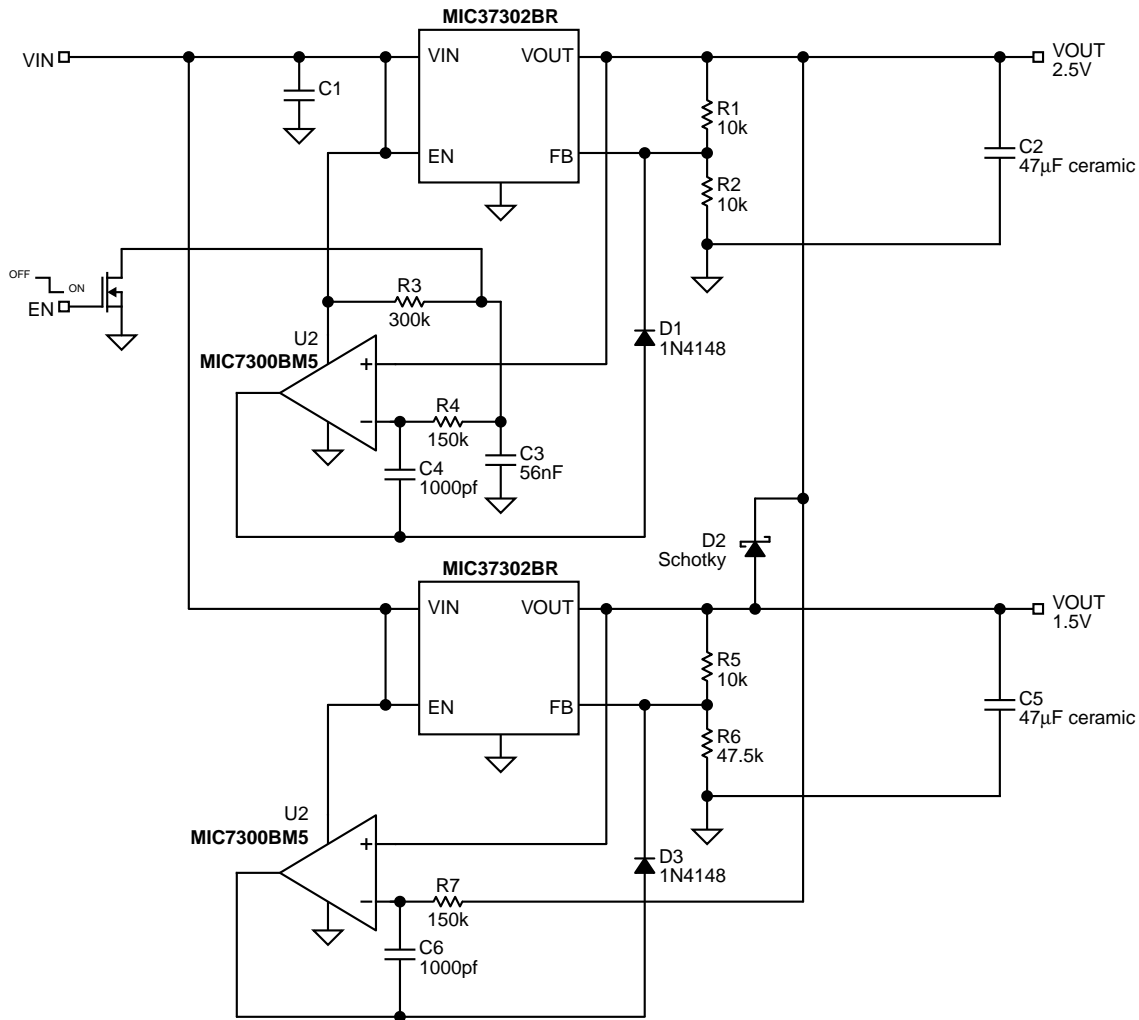


Figure 3.

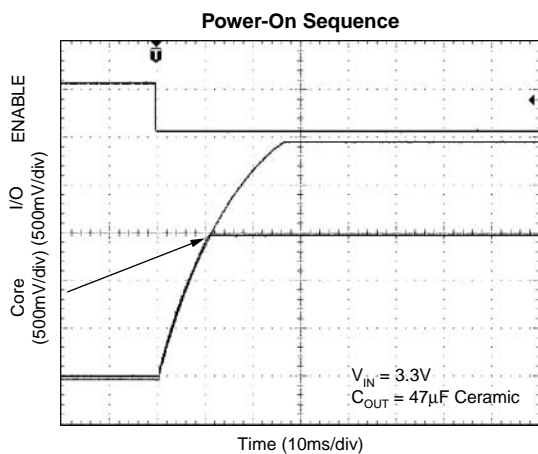


Figure 4.

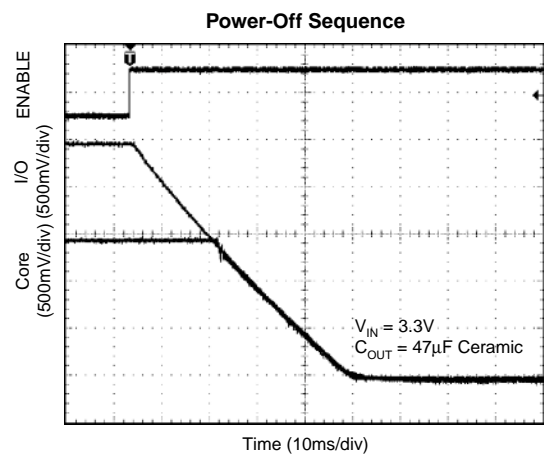


Figure 5.

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