Notes on Sensitivity and Hysteresis in Micrel Limiting Post Amplifiers

Notes on Sensitivity and Hysteresis in Micrel Limiting Post Amplifiers

Limiting post amplifiers are designed to receive low-level input signals and restore them to their standard logic levels. Applications vary, but their primary use is to receive weak signals that have been attenuated or degraded by losses in transmission through either a copper, cable or optical fiber network and restore them to useful and error free logic levels.

Micrel manufactures a family of limiting post amplifiers with special features that make them attractive to the communications industry where signal integrity is important. Not only do they amplify and restore the input signal, they can notify the network that the input signal is either lost or so low that it is no longer useable.

Sensitivity of Limiting Post Amplifiers

The sensitivity of the limiting post amplifier is determined by how weak a signal it is able to detect without incurring any loss of data. If the signal is clean and free of noise, then the sensitivity is typically sufficient to detect very small differential signals on the order of 1mV to 2mV. But the real sensitivity of the amplifier is sometimes governed by other factors such any noise that may be present along with the input signal. The sensitivity is typically defined as the smallest input signal strength that can be used without generating intolerable bit errors or the input signal strength that will generate less than a specified bit error rate. This sensitivity is not only defined by the post amplifier but by any background noise that may be present. This noise can be generated from a number of sources along a transmission path. Noise can be coupled into input externally or from a pre-driver or in an optical application, by thermal noise in a optical signal detector such as a PIN or APD diode or in the transimpedence amplifier.

Signal Detect and Loss-of-Signal

Once a desired sensitivity or useable signal strength is established, it is desirable to be able to know when the signal drops below the sensitivity of a given receiving system and is too weak to be useable. Micrel's limiting post amplifiers have features that detect and signal the presence or loss of a useable input signal. Those with signal detect (SD) output, assert a true logic level if the signal strength is sufficient enough to be useful. Those that have features detecting the Loss-of-Signal, or those with LOS output, assert a true logic level when the input signal is too weak to be useable. The sensitivity or input signal amplitude, which triggers an LOS or SD assertion, can be adjusted by setting the voltage on either the LOSLVL or SDLVL inputs, depending upon which amplifier is being used.

SD/LOS Hysteresis in Micrel Post Amplifiers

What is SD/LOS hysteresis as it pertains to a post amplifier? If this is the case, we are interested in whether an input signal is present or is lost and if there is a clear difference on whether the signal is increasing or decreasing when the signal is detected or lost. Without this differentiation, the LOS/SD output cannot reach a clear decision on whether a useable signal is present or not and will oscillate or chatter and become indeterminate. It is therefore desirable to see a clear difference between the onset of a loss of signal and when it is re-acquired or detected. It is therefore desirable to build-in hysteresis in these post amplifiers that clearly separates the two levels. Hysteresis is typically expressed in decibels (dB) and is defined as the ratio between the input signal strength where the post amplifier detects the presence of a signal and where it detects the loss of this signal.

For limiting post amplifiers, with the Loss-of-Signal feature, it is the ratio between the onset or de-assertion of the Loss-of-Signal output (LOSD) and the onset or assertion of the Loss-of-Signal output (LOSA). It is defined mathematically as:

$$\text{Hysteresis}_{\text{Voltage}} = 20\log\frac{\text{LOSD}}{\text{LOSA}} \qquad (1)$$

if defined in terms of the input voltage ratio

Post amplifiers with the signal detect feature define this in a similar manner, except inverted. It is the ratio between the onset of assertion of the signal detect output (SDA), as when the input signal amplitude increases enough to assert SD from its de-asserted state, and the onset of de-assertion of the signal detect output (SDD), as when the input signal amplitude

decreases enough to de-assert SD from its asserted state. It is defined mathematically as:

$$Hysteresis_{Voltage} = 20\log\frac{SDA}{SDD} \quad (2)$$

As defined in terms of the input voltage ratio

Micrel post amplifiers are typically designed to have between 2dB and 6dB of electrical voltage hysteresis.

Method for Setting the LOS/SD Sensitivity of Micrel Post Amplifiers

Micrel post amplifiers have the capability to set the LOS/SD assert/de-assert sensitivity by setting the DC voltage level on the LOSLVL or SDLVL input. In actuality, the sensitivity is set by defining the voltage difference between an on board reference voltage (V_{REF}) and the LOSLVL or SDLVL pins. Using a voltage divider between VCC and VREF, and connecting the center point of the divider to the LOSLVL or SDLVL input as shown in Figure 1.

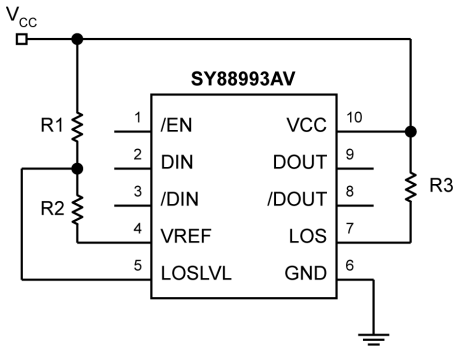


Figure 1. Typical Schematic of the Post Amplifier Showing Resistive Divider which Sets LOS/SD Sensitivity

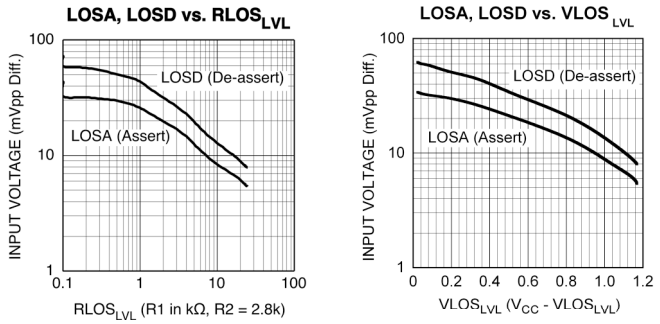
Adjusting the divider ratio sets the voltage on LOS/SDLVL:

$$V_{LOS/SDLVL} = V_{CC} - (V_{CC} - V_{REF})\frac{R1}{R1+R2} \quad (3)$$

Where V_{CC}-V_{REF} is typically 1.3V:

Micrel's post amplifier data sheets have graphs that show the input sensitivity to assert/de-assert LOS or SD as a function of the LOS/SDLVL voltage with respect to V_{CC}. Some post amplifiers have the resistor designated as R2 in Figure 1 built internal to the device. Its value is typically 2.8kΩ and the sensitivity in this case can be set with a single R1 resistor using Equation 3 and substituting R2 with 2.8kΩ. These post amplifiers, such as the SY88973V, also show the input sensitivity to assert/de-assert LOS or SD as a function of the resistor value for R1, also known as RLOSLVL or RSDLVL.

Figure 2 shows these two graphs for a device with an LOS output; the SD graphs are exactly the same, except that the LOS assert curve (the dashed line in Figure 2) becomes the SD de-assert curve and the LOS de-assert curve (the solid line in Figure 2) becomes the SD assert curve.



(a) $RLOS_{LVL}$ **(b) $VLOS_{LVL}$**

Figure 2. Input Amplitude Required to Assert/De-assert LOS vs. $RLOS_{LVL}$ (a) or $VLOS_{LVL}$ (b)

As can be seen in Figure 2, the closer the LOSLVL or SDLVL voltage is adjusted toward V_{REF} (or away from V_{CC}), the more sensitive the device becomes and the smaller or weaker the input signal amplitude can be to de-assert LOS or assert SD. As this level moves closer to V_{CC}, the less sensitive the device becomes and a larger or stronger input signal amplitude is required to de-assert LOS or assert SD. For a given LOS/SD sensitivity, the LOS/SD assert/de-assert values depend on whether LOS/SD is asserted or de-asserted, giving an inherent LOS/SD hysteresis to the device. This built-in hysteresis prevents the LOS/SD output from chattering when the input signal amplitude changes marginally from its nominal value. This hysteresis is typically 4.6dB electrical voltage for input signal voltages larger than $10mV_{pp}$, meaning that for a given input signal voltage that asserts LOS or de-asserts SD, an input signal of 1.7 times that voltage is required to de-assert LOS or assert SD. Stated in terms of optical power, the hysteresis in Micrel post amplifiers is typically 2.3dB, meaning that for a given input signal power that asserts LOS or de-asserts SD, an input signal of 1.7 times that power is required to de-assert LOS or assert SD.

In certain cases, it may be desirable to adjust the amount of hysteresis a given post amplifier might have for a given sensitivity setting. This is common in applications where the input signal strength that is being detected is very small or weak and the noise floor is relatively high with respect to the input signal. In these cases, the hysteresis can be eroded because the noise does not change in the same proportion as the signal. When this occurs, it may be desirable to have the ability

to increase the hysteresis of the device. However, not only is increased hysteresis desired, but a higher input sensitivity range may also be obtained (lower than $10mV_{pp}$), as is required when detecting very low-level or noisy input signals which can be encountered in long-haul applications.

Method for Improving the Hysteresis Sensitivity and Magnitude for an OC-TTL LOS/SD Post Amplifier

Setting the sensitivity and modifying the magnitude of the LOS/SD hysteresis can be realized on Micrel post amplifiers that feature an open-collector TTL (OC-TTL) LOS or SD output. By adding a feedback resistor (RFDBK) between the LOS output and the LOSLVL input, as shown in Figure 3, the LOSLVL can be adjusted as a function of whether LOS is asserted high or de-asserted low, thus improving the hysteresis.

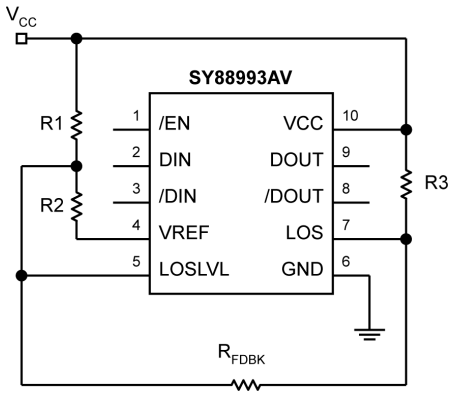


Figure 3. Increasing the Hysteresis of the Post Amplifier Using a Feedback Resistor on Devices with OC-TTL LOS

When a valid input signal is present, the feedback resistor pulls LOSLVL lower (away from V_{CC} and towards V_{REF}), increasing the sensitivity of the LOS assert trigger point. The effect of the adjustment is an inverse function of the feedback resistor RFDBK. The higher the value of the feedback resistor, the less effect it has on the hysteresis. Likewise, the lower the value of the feedback resistor, the more effect it has on increasing the hysteresis.

Similarly, when an invalid input signal is present, the feedback resistor, in parallel with the pull-up resistor R1, pushes LOSLVL higher (toward V_{CC} and further from V_{REF}), decreasing the sensitivity of the LOS de-assert trigger point. Again, this is an inverse function of the feedback resistor, but also a function of the pull-up resistor R1, which now acts as if it is in parallel with RFDBK to V_{CC}. Thus, the higher the value of R1, the more effect it has on increasing the hysteresis. Conversely, the lower the value of R1, the less effect it has on the hysteresis. It must be noted that in using this scheme, LOSLVL must be set by using a resistive voltage divider, and not a fixed voltage, so that LOSLVL can vary depending upon the state of LOS.

If the designer wishes to incorporate the hysteresis magnitude and sensitivity improvement scheme described above, a design kit is available to help choose the optimal values for R1, R2 and RFDBK. Please contact: hbwhelp@micrel.com to obtain a Microsoft Office document entitled, "Hysteresis Feedback Resistor Calculator" which describes the feedback resistor's operation in detail and provides a spreadsheet to calculate the required resistor values.

A similar technique can be used to increase the hysteresis in Micrel post amplifiers that have an OC-TTL SD output. However, in this case, an inverter consisting of field effect transistor (FET) Q1 and resistor R4 are necessary to convert the SD output into an LOS output, as shown in Figure 4. The circuit then operates as described earlier for the LOS output post amplifier.

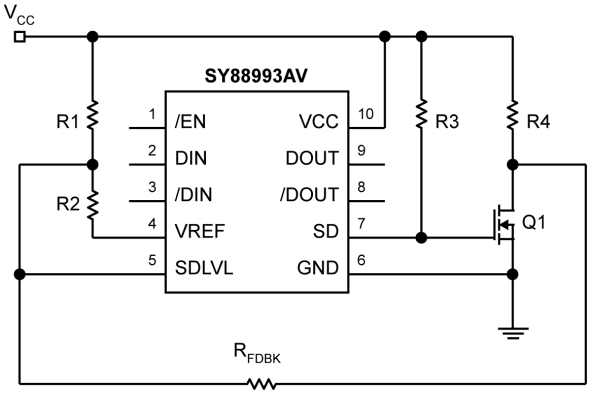


Figure 4. Increasing the Hysteresis of the Post Amplifier Using a Feedback Resistor on Devices with OC-TTL SD

Micrel's Limiting Post Amplifier Family

We have discussed at length a procedure for setting system sensitivity and increasing the LOS or SD hysteresis to improve performance in a low signal strength or noisy environment. Using these techniques, the user can improve both the LOS/SD sensitivity and the LOS/SD hysteresis to allow operation in the 5mV and below region.

Micrel has provided the greatest flexibility to its customers by providing Post Amplifiers with CML or PECL outputs, LOS or SD options, on-or-off chip input terminations and integrations of R2 and R3 on chip.

Micrel is continuing to develop improved versions of its family of limiting post amplifiers that operate at even higher frequencies, at higher input sensitivities and to improve hysteresis at their most sensitive regions of operation. Table 1 outlines a representative grouping of Micrel's current family of limiting post amplifiers.

For further information, visit www.micrel.com or contact hbwhelp@micrel.com.

Product Number	I/O Logic Type	LOS/SD PECL/TTL(1)	Bit Rate	Integrated 50Ω Input Termination	Integrated R2 and R3 On-Chip(2)
SY88933	PECL	SD/TTL	155Mbps to 1.25Gbps	No	R3 = 6.7k
SY88913	PECL	SD/PECL	155Mbps to 1.25Gbps	No	Neither Installed
SY88903	PECL	LOS/TTL	155Mbps to 1.25Gbps	No	Neither Installed
SY88923	PECL	LOS/TTL	155Mbps to 2.5Gbps	No	Neither Installed
SY88993	CML	LOS/TTL	155Mbps to 3.2Gbps	No	Neither Installed
SY88773	CML	LOS/TTL	155Mbps to 3.2Gbps	No	R2 = 2.8k, R = 4.7k
SY88973	CML	LOS/TTL	155Mbps to 3.2Gbps	Yes	R2 = 2.8k, R = 4.7k
SY88843	CML	SD/TTL	155Mbps to 3.2Gbps	Yes	R2 = 2.8k, R = 4.7k
SY88823	CML	SD/TTL	155Mbps to 3.2Gbps	No	R2 = 2.8k, R = 4.7k

Table 1. Post Amplifier Summary

Notes:

1. Figure 1 shows R2 and R3.
2. Devices with LOS have active low enable (/EN) while devices with SD have active high enable (EN). This feature can be used to cut-off or squelch the output when an input signal is not detected by tieing the LOS/SD outputs to the appropriate EN, /EN.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http:/www.micrel.com