Application Note 56

Designing a Stable Control Loop in DC-DC Converters

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Introduction

This Application Note presents a methodology for designing a stable control loop in a DC-to-DC converter. A lot of trial and error has been used try to stabilize the control loop of a DC-to-DC converter. Designing the compensation network can be a mystery if one does not know where to place the poles and zeros of the error amplifier and how much gain is needed of the error amplifier.

As switching frequencies increase so does the bandwidth of the feedback signal. The feedback signal bandwidth is usually at least 1/10 to 1/5 the switching frequency. The bandwidth of the feedback signal is determined by measuring the crossover frequency of the open loop transfer function. The frequency where the open loop transfer function is at unity gain is called the crossover frequency. With switching frequencies in the MHz's it is not uncommon to have cross over frequencies (F_{CO}) of the open loop gain in the 100's of kHz. Regardless of the operating frequency of a DC-to-DC converter, this method will provide excellent results.

A regulated switching power supply has a controlled output by means of a negative feedback system. Because feedback is present in a DC-to-DC converter there is the possibility for oscillation (instability). Any system containing feedback will oscillate under certain conditions. It is essential to know when and under what conditions the system will remain stable.

Feedback Theory

It is important to know the criteria necessary for a feedback system to remain stable; therefore one needs to look at feedback theory to gain some insight. Figure 1 illustrates a system with negative feedback.

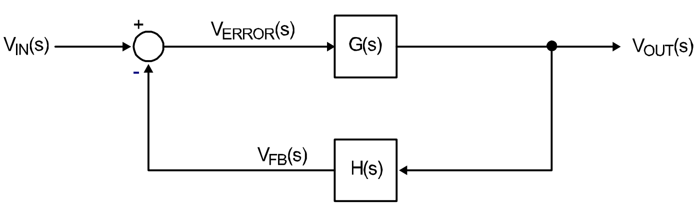

Figure 1.

The closed loop transfer function is:

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{G(s)}{1+G(s)H(s)} = \frac{G(s)}{1+T(s)}$$

When $1+G(s)H(s)=0$ The system is clearly unstable.

Therefore, the condition $G(s)H(s) \neq -1$ is one criteria for stability.

$G(s)H(s)=T(s)$ is called the open loop transfer function.

$|T(s)|$ is the magnitude of the open loop gain or sometimes called the loop gain.

IMPORTANT: || is the magnitude not the absolute value and $\angle T(s)$ is the phase of the open loop gain or simply the loop phase.

When $|T(s)|=1$ and $\angle T(s)=-180°$ the system is unstable.

The open loop gain and phase determines the stability of a system. It may seem confusing to call T(s) the open loop gain when it is a closed loop system it is describing. It can be explained as such, $G(s)H(s)$ is the product of the forward gain and the feedback gain around the loop. When $H(s)$ is non-zero, the system clearly has feedback and is therefore, describes a closed loop system.

Another criteria for a stable system is when the magnitude $|T(s)|=1$ the phase $\angle T(s) \geq -180°$.

DC-To-DC Converter Feedback System

Figure 2 shows the simplified system schematic of a voltage mode synchronous buck DC-to-DC converter such as Micrel's MIC2130/1. The internal transconductance error amplifier is used for compensating the voltage feedback loop by placing a capacitor (C1) in series with a resistor (R1) and another capacitor C2 in parallel from the COMP pin-to-ground. (Note: Ceramic output caps may require type III compensation and is the subject of a different article). The DC-to-DC converter is represented as gain blocks in Figure 3.

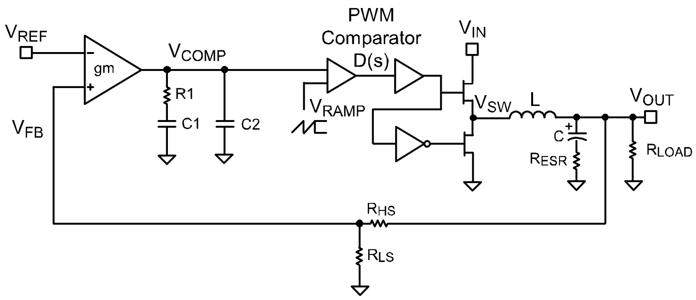

Figure 2. Simplified System Schematic

From feedback theory one of the criteria for stability is when the open loop gain T(s) = 1 $\Rightarrow$ (0db), the open loop phase $\angle T(s) \geq -180^\circ$, i.e., the phase has to be greater (less negative) than -180°. The amount the phase is greater than -180° is called the phase margin, typically 30 to 60°. Phase margin is a key parameter when predicting the stability of the system and how much overshoot and undershoot the system exhibits during transients.

The system block diagram is shown in Figure 3.

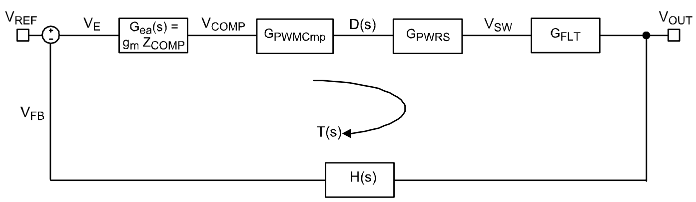

Figure 3. System Block Diagram

The open loop transfer function is:

$$T(s) = G_{ea}(s) * G_{PWMCmp}(s) * G_{PWRS}(S) * G_{FLT}(S) * H_{FB}(S)$$

Where the magnitude is:

$$|T(s)| = |G_{ea}(s)| + |G_{PWMCmp}(s)| + |G_{PWRS}(S)| + |G_{FLT}(S)| + |H_{FB}(s)|$$

And the phase is:

$$\angle T(s) = \theta_T(s) = \theta_{ea} + \theta_{PWMComp} + \theta_{PWRS} + \theta_{FLT} + \theta_{FB}$$

In the system block diagram in Figure 3:

$G_{ea}(s) = \dfrac{\Delta V_{comp}}{\Delta V_{error}} = gm * Z_{comp}$ Gain of the transconductance type error amp.

For the specific case of the MIC2130 family of controllers, g_m = 1.5ms and $Z_{comp}(s) = \left(R1 + \dfrac{1}{sC_1}\right) \| \left(\dfrac{1}{sC_2}\right)$

$G_{PWMCmp}(s) = \dfrac{\Delta D}{\Delta V_{comp}} = \dfrac{D_{max}}{\Delta V_{ramp}} = \dfrac{0.85}{2.1 - 1.1} = 0.85$ Gain of the PWM comparator.

(The MIC2130/1 has a Max duty = 85% which corresponds to ΔV_{comp} = 1V).

$G_{PWRS}(s) = \dfrac{\Delta V_{SW}}{\Delta_D(s)} = \dfrac{V_{OUT}}{\Delta_D(s) * D} = \dfrac{V_{OUT}}{D_{max} * D}$ Gain of the Power Stage.

$G_{FLT}(s) = \dfrac{\Delta V_{OUT}}{\Delta V_{SW}} = \dfrac{1 + sR_{ESR}C_{OUT}}{1 + \dfrac{s}{Q\varpi_0} + \dfrac{s^2}{\varpi_0^2}}$ Gain of the filter

Where $Q = \dfrac{E_{STORED}}{E_{LOST}} = \dfrac{R_{LOAD}}{\sqrt{L/C_{OUT}}}$ (This Q is for parallel load meaning R_{LOAD} is in parallel with the output filter)

And

$\varpi_0 = \dfrac{1}{\sqrt{LC_{OUT}}}$ $F_O = \dfrac{1}{2\pi\sqrt{LC_{OUT}}}$ $F_{ESR} = \dfrac{1}{2\pi R_{ESR}C_{OUT}}$

$H(s) = \dfrac{R_{LS}}{R_{LS} + R_{HS}} = \dfrac{V_{REF}}{V_{OUT}}$ Gain of the feedback network.

For simplicity, combine the PWM comparator gain and the Power stage gain and call it the modulator gain. Therefore;

$$G_{MOD}(s) = G_{PWMCmp}(s) * G_{PWRsw}(s) = \frac{D_{max}}{\Delta V_{RAMP}} * \frac{V_{OUT}}{D * D_{max}} = \frac{V_{OUT}}{\Delta V_{RAMP} * D}$$

$$\frac{V_{OUT}(s)}{V_{COMP}(s)} = G_{MOD}(s) * G_{FLT}(s)$$

$$T(s) = G_{ea}(s) * G_{MOD}(s) * G_{FLT}(s) * H_{FB}(s)$$

And the magnitude is:

$$|T(s)| = |G_{ea}(s)| + |G_{MOD}(s)| + |G_{FLT}(s)| + |H_{FB}(s)|$$

And the phase is:

$$\angle T(s) = \theta_T(s) = \theta_{ea} + \theta_{MOD} + \theta_{FLT} + \theta_{FB}$$

Where $\theta_{ea} = -\theta_{POLE0} + \theta_{ZERO1} - \theta_{POLE1}$

θ_{POLE0} = phase lead due to the pole at the origin

θ_{ZERO1} = phase lead due to ZERO1

θ_{POLE1} = phase lead due to POLE1

$\theta_{PWMCmp} = 0^\circ, \theta_{PWRS} = 0^\circ, \theta_{FB} = 0^\circ$ therefore $\theta_{MOD} = 0^\circ$

The phase of the output filter includes the complex poles of L and the output capacitance C_{OUT}. At the higher frequencies there is a phase boost by the zero generated by the ESR of the C_{OUT}.

The filter has 2 poles at F_0 and a zero at F_{ESR}

$\theta_{FLT} = -180^\circ$ at F_0 and +90° at F_{ESR}

Major Steps for Designing a Stable DC-to-DC Converter

1. Use a network analyzer to measure and plot the modulator & filter gain,

$$\frac{V_{OUT}}{V_{COMP}} = G_{MOD}(s) * G_{FLT}(s)$$

2. From the plot find the gain at the desired cross over frequency F_{CO} (select a F_{CO} 1/10 to 1/5 of the switching frequency)
3. Having found $G_{MOD}(s)$ * $G_{FLT}(s)$ and knowing the feedback gain H(s). Determine the required error amp gain $G_{ea}(s) = \frac{\Delta V_{COMP}}{\Delta V_{ERROR}} = g_m * Z_{COMP}(s)$ so the open loop gain at F_{CO} is 0db.

$$|T(2\pi F_{CO})| = 0db = |G_{ea}(2\pi F_{CO})| + |G_{MOD}(2\pi F_{CO})| + |G_{FLT}(2\pi F_{CO})| + |H_{FB}(2\pi F_{CO})|$$

$$|G_{ea}(2\pi F_{CO})| = -|G_{MOD}(2\pi F_{CO})| - |G_{FLT}(2\pi F_{CO})| - |H_{FB}(2\pi F_{CO})|$$

IMPORTANT: || is the magnitude not the absolute value.

4. Design the error amp gain with enough gain at F_{CO} so the open loop gain is 0db at F_{CO}.
5. Locate the poles and zero of the error amp for the desired phase margin.

Example:

The MIC2130 family of controllers is used as an example.

V_{IN} = 24V; V_{OUT} = 3.3V; I_{OUT} = 10A; L = 7.3µH; C_{OUT} = 670µF; R_{ESR} = 40mΩ; F_{SW} = 150kHz

The gain and phase of the modulator and filter is:

$$\frac{V_{OUT}(s)}{V_{COMP}(s)} G_{MOD}(s) * G_{FLT}(s)$$ (see Figure 2).

A computer generated plot of $\frac{V_{OUT}(s)}{V_{COMP}(s)} G_{MOD}(s) * G_{FLT}(s)$ is shown in Figure 4.

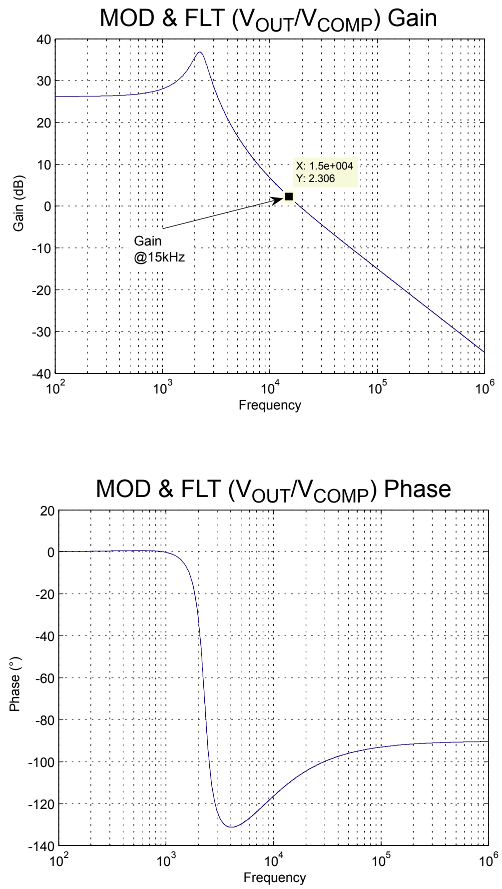

Figure 4. Modulator Transfer Function

There is a –180° phase change near F_0. At frequencies greater than F_0 the phase increases towards –90° due to the zero of F_{ESR}. The phase effects of poles and zeros start a decade below and finish a decade above. Therefore, at the frequency of a pole or zero the phase effect is only half of the final value. At the complex pole 2.3kHz the phase is –90° and would be –180° at 23kHz if not for the +90° phase lead of the zero at around 6kHz due to the ESR of the filter capacitors. (Actually, the phase gain plots reach their final values asymptotically).

By inspecting Figure 4 the DC and low frequency gain of

$$G_{MOD}(0) = \frac{V_{OUT}}{\Delta V_{RAMP} * D} = \frac{3.3}{1 * 3.3/24} = 24 \Rightarrow 27.6dB$$

F_0 = 2.3kHz; F_{ESR} = 6kHz and Q is 10dB.

The peak Gain equals the low frequency gain plus the Q ≈ 27 + 10 ≈ 37dB.

It is desired that T(s) have a cross over frequency (F_{CO}) of 1/10 the Switching frequency ≈ 15kHz. It is required that $\angle T(j2\pi F_{CO})$ be greater than –180° by at least the phase margin. By inspecting the Gain plot of $G_{MOD}(s) * G_{FLT}(s)$ at 15kHz the gain is about 2.3dB.

Therefore, to make $T(2\pi F_{CO}) = 1 \Rightarrow$ 0dB;

$T(s) = G_{ea}(s) * G_{MOD}(s) * G_{FLT}(s) * H_{FB}(s) = 1 \Rightarrow 0dB$ at F_{CO}

$H_{FB} = V_{REF} / V_{OUT} = 0.7/3.3 = 0.212 \Rightarrow -13.5dB$

$|G_{ea}|_{dB} = |T|_{dB} - |G_{MOD}|_{dB} - |H_{FB}|_{dB} = 0 - 2.3dB - (-13.5dB) =$ $11.2dB \Rightarrow 3.63$ the error amp needs 11.2dB of gain at F_{CO}.

Therefore, $g_m * Z_{COMP}$ = 3.63 at 15kHz.

The error amp's mid band (flat part) should be centered at the desired cross over frequency (see Figure 5) this will give the maximum phase boost. The location of the error amp's zero and poles are selected in order to achieve the desired phase margin of T(s). For the maximum phase boost at the cross over Frequency (F_{CO}), place the first Zero1 of the EA at F_{CO}/10 since the effect of its phase boost will be at the maximum at F_{CO}. Likewise, place the pole of the EA at least 10 x F_{CO} so the effects of its phase lag will be at a minimum at F_{CO} and the mid band gain at 11.2db. Therefore, using the standard values: R1 = 243k; C1 = 0.047µF; C2 = 470pF.

g_m Error Amplifier

Usually, it is undesirable to have high error amplifier gain at high frequencies. Otherwise, high frequency noise spikes at large amplitude would be present at the output. Hence, gain should be permitted to fall off at high frequencies. At low frequency, it is desired to have high open-loop gain for good regulation and to attenuate power line ripple. Thus, the error amplifier gain should be allowed to increase rapidly at low frequencies.

The transfer function for the internal g_m error amplifier with R1, C1, and C2 at the comp pin is given by the following equation:

$$G_{ea}(s) = g_m \cdot \left[\frac{1 + sR1C1}{s(C1 + C2) \cdot \left(1 + R1 \cdot \frac{sC1C2}{C1 + C2}\right)} \right]$$

The above equation can be simplified by assuming C2<<C1,

$$G_{ea}(s) = g_m \cdot \left[\frac{1 + sR1C1}{s(C1) \cdot (1 + R1C2)} \right]$$

From the above transfer function, one can see that R1 and C1 introduce a zero and R1 and C2 introduce a pole at the following frequencies:

$F_{ZERO1} = 1/[2\pi * R1 * C1]$ $\quad F_{POLE1} = 1/[2\pi * C2 * R1]$

$F_{POLE@ORIGIN} = 1/[2\pi * C1]$

Figure 5 shows the gain and phase curves for the above transfer function with R1 = 2.43k, C1 = 0.047µF, C2 = 470pF, and g_m = 0.0015Ω–1. It can be seen that at 15kHz, the error amplifier exhibits approximately 11.2db of gain and 170° of phase. Figure 6 shows the open loop transfer function T(s) with these component values. It has a cross over frequency of 15KHz and phase margin of 60˚

Figure 7 shows all the gains together. As can be seen

$T(s) = G_{ea}(s) * G_{MOD}(s) * G_{FLT}(s) * H_{FB}(s)$

The magnitude of the open loop transfer function equals the sum of the magnitude of the gain blocks around the loop. And the phase of the open loop transfer function equals the sum of the phase of the gain block around the loop.

$|T(s)| = |G_{ea}(s)| + |G_{MOD}(s)| + |G_{FLT}(s)| + |H_{FB}(s)|$

and $\angle T(s) = \theta_T(s) = \theta_{ea} + \theta_{MOD} + \theta_{FLT} + \theta_{FB}$.

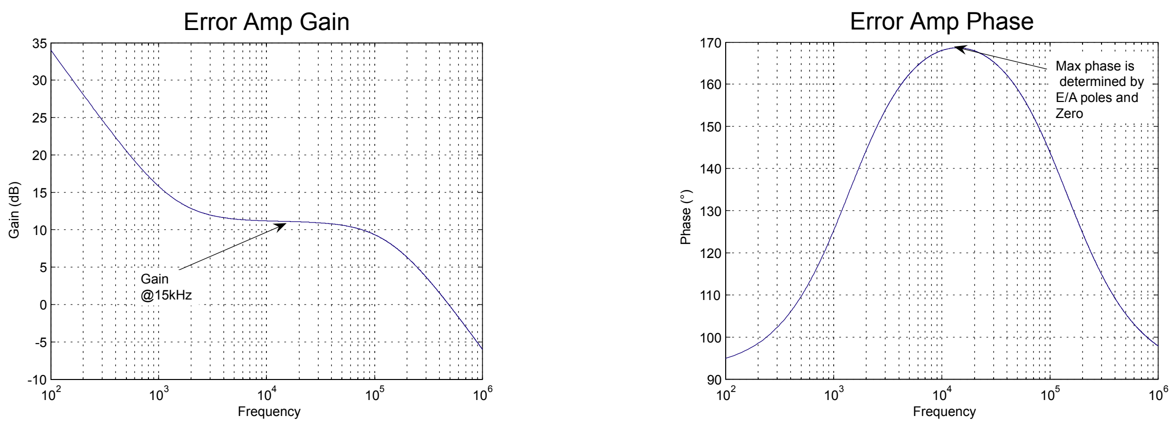

Figure 5. Error Amp Gain and Phase

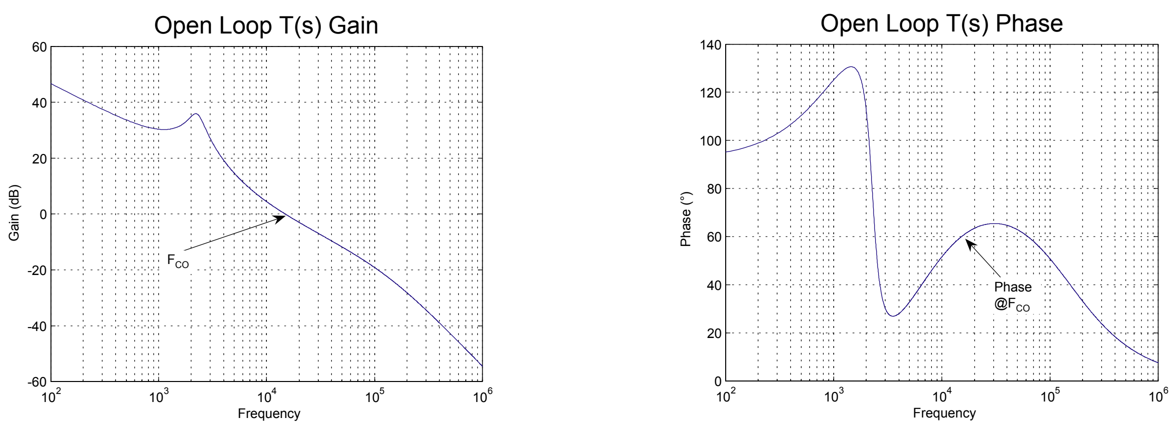

Figure 6. The Open Loop T(s) Gain and Phase

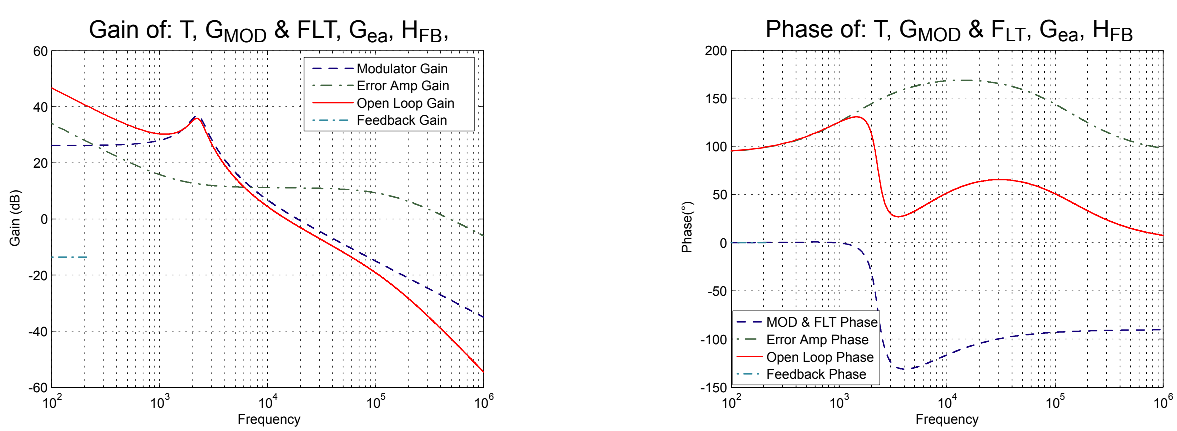

Figure 7. Gain and Phase of: T(s), G_{ea}(s), G_{MOD}(S), G_{FLT}(S), H_{FB}(s)

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