

General Description

This application note highlights the differences between the KS8695 and the KS8695X, and attempts to assist the designer who is familiar with the KS8695 transition to the KS8695X.

The KS8695 was the industry's first system-on-a-chip with an ARM9™ processor and an embedded 5-port managed switch. The popularity of the KS8695 in the SOHO market to address wireline router and gateway applications led to the development of the KS8695X, which is more optimized as a specialty part for this type of application.

External MAC Interface

The main functional difference between the KS8695 and the KS8695X is the absence of the external MAC (EMAC) MII interface on the KS8695X. This difference is shown in the block diagrams below. Most wireline router applications do not use an external MAC interface, making the KS8695X a more optimized solution.

The pins that supported the EMAC interface are now considered test pins and do not need to be connected for operation. Table 1 shows the pins that have changed in the KS8695X.

Pin Number	Signal on KS8695	Signal on KS8695X
84	MPMSEL	TEST3
130	MTXC	TEST4
131	MTXD[3]	TEST5
132	MTXD[2]	TEST6
133	MTXD[1]	TEST7
134	MTXD[0]	TEST8
135	MTXEN	TEST9
136	MTXER	TEST10
139	MCRS	TEST11
140	MCOL	TEST12
141	MRXC	TEST13
142	MRXD[3]	TEST14
143	MRXD[2]	TEST15
144	MRXD[1]	TEST16
145	MRXD[0]	TEST17
146	MRXDV	TEST18
147	MRXER	TEST19

Table 1. KS8695X EMAC Pin Changes

Since the EMAC interface has been removed in the KS8695X, the corresponding registers have also been removed, as shown in Table 2.

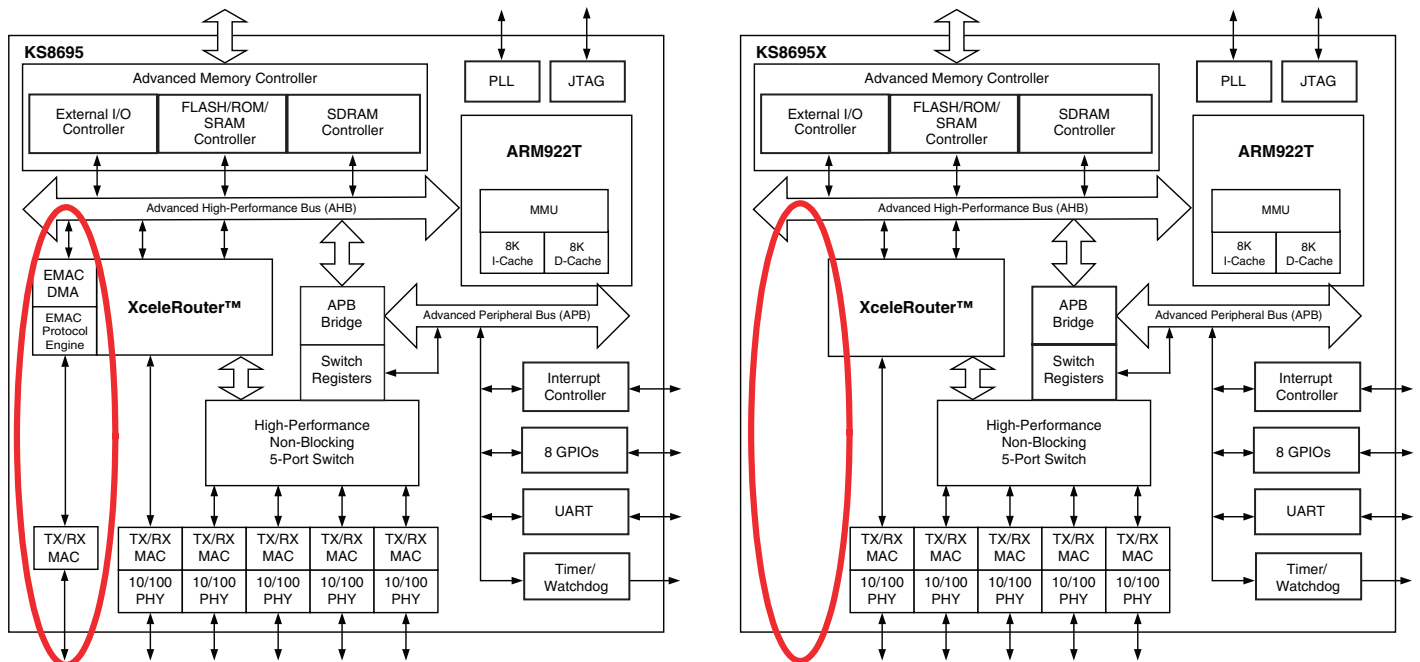


Figure 1. KS8695M Gateway Configuration

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Registers	KS8695 Register Offset	KS8695X Register Offset	Notes
Interrupt Controller Registers			
Interrupt Mode Control Register	0xE200	0xE200 (reserve bit 23:18)	Reserve EMAC related bits.
Interrupt Enable Register	0xE204	0xE204 (reserve bit 23:18)	Reserve EMAC related bits.
Interrupt Status Register	0xE208	0xE208 (reserve bit 23:18)	Reserve EMAC related bits.
Interrupt Priority Register for EMAC	0xE210	Removed	
Interrupt Mask Status Register	0xE22C	0xE22C (reserve bit 23:18)	Reserve EMAC related bits.
Interrupt Pending Highest Priority Register for FIQ	0xE230	0xE230 (reserve bit 23:18)	Reserve EMAC related bits.
Interrupt Pending Highest Priority Register for IRQ	0xE234	0xE234 (reserve bit 23:18)	Reserve EMAC related bits.
Switch Engine Registers			
Switch Engine Control 0 Register	0xE800	0xE800 (change default values for bit 27:22)	Default values changed for KS8695X: bit 27:25 = 0x0 bit 24:22 = 0x6
EMAC DMA Registers			
EMAC DMA Transmit Control	0xA000	Removed	
EMAC DMA Receive Control	0xA004	Removed	
EMAC DMA Transmit Start Command	0xA008	Removed	
EMAC DMA Receive Start Command	0xA00C	Removed	
EMAC Transmit Descriptor List Base Address	0xA010	Removed	
EMAC Receive Descriptor List Base Address	0xA014	Removed	
EMAC Station Address Low Register	0xA018	Removed	
EMAC Station Address High Register	0xA01C	Removed	
ADD MAC Low 0	0xA080	Removed	
ADD MAC High 0	0xA084	Removed	
ADD MAC Low 1	0xA088	Removed	
ADD MAC High 1	0xA08C	Removed	
ADD MAC Low 2	0xA090	Removed	
ADD MAC High 2	0xA094	Removed	
ADD MAC Low 3	0xA098	Removed	
ADD MAC High 3	0xA09C	Removed	
ADD MAC Low 4	0xA0A0	Removed	
ADD MAC High 4	0xA0A4	Removed	
ADD MAC Low 5	0xA0A8	Removed	
ADD MAC High 5	0xA0AC	Removed	
ADD MAC Low 6	0xA0B0	Removed	
ADD MAC High 6	0xA0B4	Removed	

Registers	KS8695 Register Offset	KS8695X Register Offset	Notes
ADD MAC Low 7	0xA0B8	Removed	
ADD MAC High 7	0xA0BC	Removed	
ADD MAC Low 8	0xA0C0	Removed	
ADD MAC High 8	0xA0C4	Removed	
ADD MAC Low 9	0xA0C8	Removed	
ADD MAC High 9	0xA0CC	Removed	
ADD MAC Low 10	0xA0D0	Removed	
ADD MAC High 10	0xA0D4	Removed	
ADD MAC Low 11	0xA0D8	Removed	
ADD MAC High 11	0xA0DC	Removed	
ADD MAC Low 12	0xA0E0	Removed	
ADD MAC High 12	0xA0E4	Removed	
ADD MAC Low 13	0xA0E8	Removed	
ADD MAC High 13	0xA0EC	Removed	
ADD MAC Low 14	0xA0F0	Removed	
ADD MAC High 14	0xA0F4	Removed	
ADD MAC Low 15	0xA0F8	Removed	
ADD MAC High 15	0xA0FC	Removed	
EMAC Misc. Control Register	0xEA08	Removed	
WAN Misc. Control Register	0xEA0C	0xEA0C (change default values for bit 2:0)	Default values changed for KS8695X: bit 2:0 = 0x6

Table 2. Register Differences Between the KS8695 and KS8695X

Porting Micrel KS8695 Linux Software to the KS8695X

The absence of the external MAC interface in the KS8695X affects initialization and Ethernet driver code in Micrel's Linux software. The software in the KS8695X evaluation kit CD ROM has been upgraded. Initialization code changes can be found by searching file `.\loader\diag\diag.c` for KS8695X. In this file, the external MAC interface is referred to as EMAC. Ethernet driver code changes can be found by searching the following files: `.\linux\drivers\net\ks8695\ks8695_fxhw.c` and `.\linux\drivers\net\ks8695\ks8695_main.c` for KS8695X. In these files, the external MAC interface is referred to as HPNA.

KS8695X initialization and Ethernet driver code must not access the following external MAC interface related registers and register fields:

```

REG_EMAC_DMA_TX           0xA000
REG_EMAC_DMA_RX           0xA004
REG_EMAC_DMA_TX_START     0xA008
REG_EMAC_DMA_RX_START     0xA00C
REG_EMAC_TX_LIST          0xA010
REG_EMAC_RX_LIST          0xA014
REG_EMAC_MAC_LOW         0xA018
REG_EMAC_MAC_HIGH        0xA01C

```

```

REG_EMAC_BIST              0xA07C
REG_EMAC_MAC_ELOW         0xA080
REG_EMAC_MAC_EHIGH        0xA084
REG_INT_EMAC_PRIORITY     0xE210

KS8695_INT_ENABLE         0xE204 (register fields
                             defined below)

INT_HPNA_TX               0x00800000
INT_HPNA_RX               0x00400000
INT_HPNA_TX_UNAVIAL       0x00200000
INT_HPNA_RX_UNAVIAL       0x00100000
INT_HPNA_TX_STOPPED       0x00080000
INT_HPNA_RX_STOPPED       0x00040000

REG_MISC_CONTROL          0xEA08 (register fields
                             defined below)

FULL_DUPLEX               0x00000001
SPEED_100                 0x00000002

```

PHY And Voltages

In addition to removing the external MAC interface in the KS8695X and improving the physical layer transceivers, the amount of voltage required is decreased. For the PHY, the clock and data recovery circuits have been enhanced to make them more robust when receiving ill-conditioned Ethernet signals. This means that the end product can operate in less favorable conditions in the field, whether it be old Ethernet wiring or a link partner that transmits a signal outside of IEEE specifications.

The voltage supply requirements in the KS8695X have also been reduced. This allows current KS8695 customers to keep their board designs and reduce the cost of LDOs on the board. In order to do this, the KS8695X is designed to accept either 3.3V or 2.5V on the V_{DDAT} pins. Table 3, on the following page, gives the voltages requirements for the KS8695 and the KS8695X.

Conclusion

The KS8695X is the optimum solution for a wireline router/gateway application. The removal of the external MAC interface, improvement in the PHY, and a reduction in voltage supply requirements make the KS8695X easier to use in addition to presenting a more cost-effective solution.

Since the external MAC interface is not used in most wireline router/gateway applications, its removal decreases the amount of traces that need to be routed, making it easier to route economic 2 layer boards. Removing the external MAC interface also results in less register configuration at boot time as well as a small power reduction in the chip.

The PHY improvement allows raises the customer confidence ensuring that the KS8695X-based product will perform under non-ideal conditions in the field. Aging legacy Ethernet equipment and old wiring in the field may deliver signalling that has drifted out of IEEE specification. The new improvements in the clock and data recovery circuits in Micrel's PHYs allow for the KS8695X to perform more robustly in these type of environments.

Finally, the reduction in voltage supply requirements has been engineered to make the KS8695X backward compatible with the KS8695. This backward compatibility allows current KS8695 customers to use their existing boards with the KS8695X and thus reduce their BOM cost by removing LDOs and power circuitry. Customers using the KS8695X in new designs will only be required to provide two voltages. With these new features, KS8695X is truly the most optimized and easy-to-design solution for wireline gateway applications.

Pin Number	Pin Name	Type	Pin Function
152	VDDA-PLL	1.8V Analog VDD for PLL	1.8V Analog VDD for PLL
173 179	VDDAT	2.5V Analog VDD	2.5V or 3.3V Analog VDD
154 157 170 186 193 195	VDDAR	1.8V Analog VDD	1.8V Analog VDD
25 43 90 115 128	VDD-CORE	2.0V Digital Core VDD	1.8V Digital Core VDD
1 11 21 34 47 53 63 73 79 103 137	VDD-IO	3.3V Digital I/O Circuitry VDD	3.3V Digital I/O Circuitry VDD
26 44 91 116 129	VSS-CORE	Digital Core VSS	Digital Core VSS
2 12 22 35 48 54 64 74 80 104 138	VSS-IO	Digital I/O VSS	Digital I/O VSS
153 155 156 161 164 167 171 176 182 185 189 192 194 196	GNDA	Analog Ground	Analog Ground

Table 3. KS8695 Versus KS8695X Voltage Requirements

For additional support, contact your local Micrel Field Application Engineer or salesperson.

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