



General Description

KS8993 is a three-port, integrated 10/100 switch, and has uses in 100BASE-FX to 10/100BASE-TX Media Converter applications. The KS8993I is the industrial temperature (-40°C to +85°C) version.

This application note describes how to interface the KS8993 100BASE-FX port with a LVPECL/PECL fiber transceiver.

Please contact your local Micrel FAE or salesperson if you have any questions.

100BASE-FX Configuration

The KS8993 have three fiber signal detect pins:

FXSD1: pin #127

FXSD2: pin #36

FXSD3: pin #37

If $FXSDx > 0.6$ Volts (V), the physical port runs in 100BASE-FX mode. If $FXSDx$ is shorted to ground, the physical port runs in TX mode.

Since there is no auto-negotiation standard for fiber mode, the speed (100FX) and duplex (Full) need to be configured for each port. Configurations are set by boot-strapping the appropriate KS8993 pins with pull-ups. Please refer to the KS8993 data sheet for further details.

Once 100BASE-FX mode is enabled, the KS8993 compares the input voltage level going into the $FXSDx$ pin with the $VREFx$ pin voltage level reference to determine if there is a signal or a Far End Fault (FEF) (no signal) from the fiber transceiver. Table 1 indicates the $FXSDx$ input voltage thresholds and the recommended input voltage detection levels for switching between the different modes.

Type of Mode	FXSDx (Input Voltage Threshold)	Recommended FXSDx Detection Level for $VREFx = +2.09V$
TX mode	$< 0.1V$	Ground
FX mode – No signal detected – Far-end fault generated	$> 0.6V$ $< [VREFx - 0.22V]$	$> +0.60V$ $< +1.87V$
FX mode – Signal detected	$< [VREFx + 0.03V]$	$> +2.12V$

Table 1. KS8993 FX/TX Mode Selection with the FXSDx Input Voltage Level

An FEF occurs when there is no signal detected on the receive side of the fiber transceiver. The transmission side signals the other end of the link that there is an FEF by sending 84-ones and 1-zero in the idle period between frames. The station that receives the FEF turns off its LINK status to indicate a faulty link, but continues to transmit its normal pattern.

The FEF feature can be disabled (applies to all ports) by setting the KS8993 pins as follows:

Test[1] = float and Test[2] = '0'

KS8993 FX Interface

A typical KS8993 interface to a fiber transceiver is illustrated in Figure 1. In the illustration, the KS8993 is AC-coupled to the fiber transceiver with 0.1μF capacitors, which are used to discard the DC voltage offset differences between the fiber transceiver and the KS8993 due to differing V_{CC} levels, e.g., +3.3V/+5V and +2.5V, respectively.

The recommended termination for the TX differential pair is 49.9Ω tied to the KS8993 supply voltage, +2.5V. On the received side, the termination is 100Ω across the RX differential pair. See Figure 1 on page 2.

Fiber Signal Detect

The KS8993 fiber signal detect circuit works by sensing the output voltage level from the fiber transceiver signal detect (SD) pin and comparing this level with the KS8993 $VREFx$ input voltage reference level. The SD pin will output a '1' if a signal is detected and a '0' if not.

There is a DC offset of about +90mV between $VREFx$ and $FXSDx$. To set the $FXSDx$ pin's voltage detection reference at +2.0V, $VREFx$ needs to be DC-biased to +2.09V. $VREFx$ can be DC-biased to a maximum of +2.10V. In Figure 1, RB1 and RB2 set the $VREFx$ reference voltage. To track the SD pin's output voltage variation caused by the supply voltage changes, RB1 is tied to the V_{CC} supply of the fiber transceiver.

Resistors RD1 and RD2 act as a voltage divider to translate the SD pin's PECL output voltage level to the $FXSDx$ pin's CMOS input voltage level. For LVPECL, the SD output is connected directly to the KS8993's $FXSDx$ pin if $VREFx$ is set to +2.09V. With the direct connection, a 130Ω resistor needs to be connected from the SD pin to ground. This resistor provides a DC path to sink the SD pin's open emitter transistor's output current.

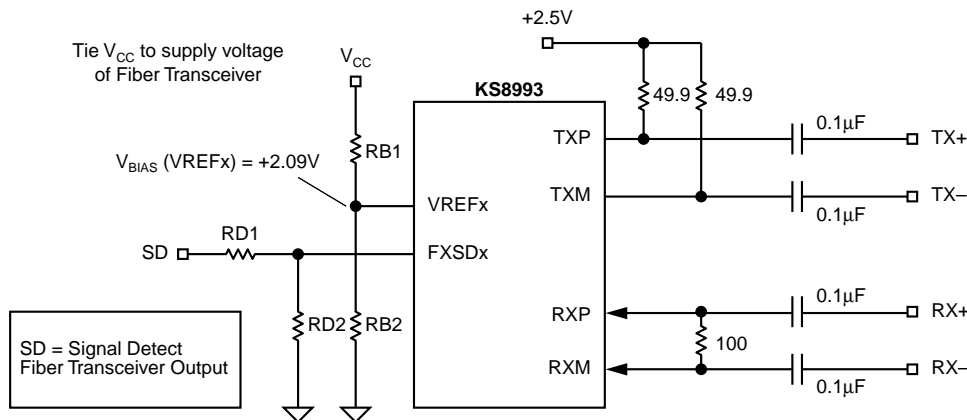


Figure 1. Typical KS8993 Interface to a Fiber Transceiver

Table 2 lists the typical resistors values for Figure 1.

For PECL fiber transceiver, the values for RD1 and RD2 in Table 2 translate the SD pin's +3.7VDC bias to the FXSDx pin's +2.0V detection reference. This translation reduces the SD output voltage level to 54% at the FXSDx pin input. Similarly, the $[V_{OH}(min) - V_{OL}(max)]$ threshold window is reduced from 570mV_{pp} to 308mV_{pp}.

Table 2 gives the recommended resistor values and the VREFx DC bias voltage for LVPECL/PECL voltage translation and DC-biasing. These resistor values may need to be changed to provide better sensitivity and sufficient threshold margin for the FXSDx pin. Refer to the fiber transceiver data sheet.

The following equations are used to compute the resistor values in Table 2:

$$V(\text{FXSDx detection reference}) =$$

$$V_{\text{bias}}(\text{SD}) \times \left[\frac{RD2}{(RD1 + RD2)} \right]$$

$$VREFx = V_{CC}(\text{fiber transceiver}) \times \left[\frac{RB2}{(RB1 + RB2)} \right]$$

$$VREFx = V(\text{FXSDx detection reference}) + 0.09V$$

	V _{CC} (V)	RD1 (Ω)	RD2 (Ω)	RB1 (Ω)	RB2 (Ω)	VREFx (DC Bias)
LVPECL	+3.3	SHORT	130	475 1%	825 1%	+2.09V
PECL	+5.0	4.75K 1%	5.62K 1%	1150 1%	825 1%	+2.09V

Table 2. Typical Resistor Values for LVPECL/PECL Voltage Translation and Biasing

Table 3 lists the standard LVPECL and PECL ranges for output voltage high/low and the DC voltage bias. Nonstandard PECL usually has a different DC voltage bias. Check the fiber

transceiver specification for the the PECL DC voltage bias and set the voltage divider accordingly by RD1 and RD2.

	Standard PECL Output Level (Reference to V _{CC})	LVPECL (V _{CC} = +3.3V)	PECL (V _{CC} = +5.0V)
V _{OH} (max)	-0.88V	+2.42V	+4.12V
V _{OH} (min)	-1.05V	+2.25V	+3.95V
V _{DC} (bias)	-1.32V	+1.98V	+3.68V
V _{OL} (max)	-1.62V	+1.68V	+3.38V
V _{OL} (min)	-1.84V	+1.46V	+3.16V

Table 3. Standard LVPECL and PECL Output Voltage Levels

Typical Configuration on Fiber Transceiver Side

Most fiber transceivers available on the market today are either LVPECL or PECL. For example, this section describes the KS8993 interface to the Agilent HFBR-5903, a LVPECL fiber transceiver.

Figure 2 illustrates a typical KS8993 interface to the Agilent HFBR-5903. LVPECL requires the DC voltage bias to be set at +2.0V. The voltage divider combination of R3 and R4 sets the required DC bias and provides 50Ω termination for the transmit differential pair, TD+/TD-. On the receive side, R5 is required to provide a DC path to sink the open emitter transistor's output current for the receive differential pair, RD+/RD-.

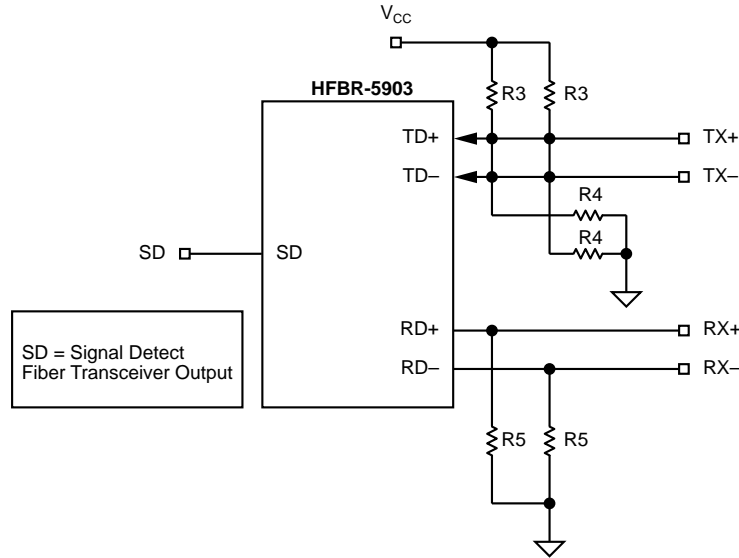


Figure 2. Typical Fiber Transceiver (HFBR-5903 Shown) Interface to the KS8993

Table 4 lists the typical resistor values for R3, R4, and R5 shown in Figure 2 and for other similar fiber transceivers that require PECL level DC biasing and termination.

The fiber transceiver signal detect output is discussed in the “Fiber Signal Detect” section. For further information, refer to the Agilent HFBR-5903 data sheet.

	V _{CC} (V)	RD3 (Ω)	RD4 (Ω)	RB5 (Ω)
LVPECL	+3.3	82	130	130
PECL	+5.0	68	191	270

Table 4. Typical Resistor Values for LVPECL and PECL Termination and DC Biasing

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