



## SY84403BL Evaluation Board

Ultra Small 3.3V, 4.25Gbps CML Limiting Post Amplifier with TTL LOS

### General Description

The SY84403BL evaluation board enables fast and thorough evaluation of the SY84403BL. Designed to be driven by a high-speed, pattern generator, the board is an easy-to-use, single supply design. The SY84403BL evaluation board is intended to terminate to a 50Ω scope and provides for simple user adjustability of the LOS threshold through the adjustment of an on-board potentiometer. The SY84403BL is part of Micrel's industry leading family of ultra small Fiber Optic ICs.

All data sheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

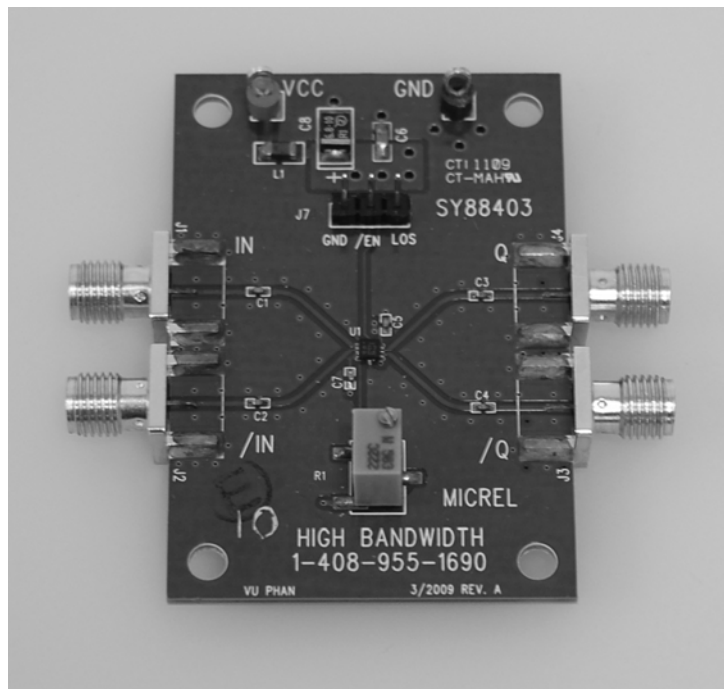
### Features

- SY84403BL: Ultra Small CML Limiting Post Amplifier with High-Sensitivity TTL LOS
- Single +3.3V power supply
- AC-coupled configuration for direct interface with 50Ω test equipment
- On-board LOS sensitivity adjustment

### Related Documentation

- SY84403BL: Ultra Small 3.3V, 4.25Gbps CML Limiting Post Amplifier with High-Sensitivity TTL LOS

### Evaluation Board



## Evaluation Board Description

The SY84403BL evaluation board is designed to operate with a single 3.3V  $\pm 10\%$  power supply and is configured with AC-coupled inputs and outputs. The high-speed input and output channels are brought out to SMA connectors through matched length AC-coupled differential strip-line traces.

### AC-Coupled Input

The AC-Coupled inputs automatically bias the input levels to the correct DC-operating point set by the VT jumper input. Therefore, the inputs can be driven by a differential signal smaller than 100mV (200mV<sub>PP</sub>) without level shifting or termination resistor network in the signal path.

### AC-Coupled Output

The SY84403BL is configured with AC-coupled outputs allowing the board to interface directly with 50 $\Omega$  equipment. AC-coupling allows the board to use a single power supply. If only one output is being used, the unused complimentary output should be terminated into 50 $\Omega$ -to-ground.

### SY84403BL AC-Coupled Evaluation Board Setup

This section explains how to connect and setup the SY84403BL evaluation board per Figure 1. Ensure proper ESD precautionary measures are taken before handling sensitive electronic equipment, including the SY84403BL evaluation board.

## Measurements

### Evaluating DOUT and /DOUT

1. Set a DC power supply to +3.3V and turn it off. Connect the positive lead to V<sub>CC</sub> post and the negative lead to GND post.
2. Connect the /EN input to the GND to enable the DOUT and /DOUT output buffers.
3. Set the desired frequency on a pattern generator with amplitude between 20mV<sub>PP</sub> and 1800mV<sub>PP</sub>. Typical data patterns are 2<sup>7</sup>-1 or 2<sup>23</sup>-1 PRBS patterns depending on the application. Since the inputs to the board are AC-Coupled, the voltage offset of the pattern generator is not significant so it can be set between GND and V<sub>CC</sub>.
4. Connect the pattern generator with differential outputs as a data source to the DIN and /DIN inputs on the SY84403BL evaluation board. Use matched length differential cables.
5. Turn the power supply on.
6. Observe the DOUT and /DOUT outputs with a 50 $\Omega$  scope. The output rise and fall times should be less than 120ps, with amplitude around 400mV (800mV<sub>PP</sub> differential).

### LOS Hysteresis Measurements

The SY84403BL evaluation board provides a potentiometer to allow for convenient adjustment of LOS<sub>LVL</sub> without the need for an extra power supply. LOS<sub>LVL</sub> taps off a potentiometer connected between V<sub>CC</sub> and V<sub>REF</sub>. V<sub>REF</sub> is a reference voltage of approximately V<sub>CC</sub> -1.3V. Hence, LOS<sub>LVL</sub> can be set to any voltage between V<sub>CC</sub> and V<sub>CC</sub>-1.3, as specified in the SY84403BL data sheet. The potentiometer creates a voltage divider. Thus,

$$\text{LOS}_{\text{LVL}} = V_{\text{CC}} - \left[ \frac{1.3 \times R(\text{k}\Omega)}{R(\text{k}\Omega) + 2.8\Omega} \right]$$

Where R is the resistance of the potentiometer from V<sub>CC</sub> to the tap at LOS<sub>LVL</sub>, the steps below show how to measure the LOS hysteresis as a function of the input voltage swing at the DIN and /DIN inputs:

### Minimum Input Swing Hysteresis Measurement

The minimum acceptable input swing for the SY84403BL is 20mV<sub>PP</sub>.

7. Set a DC power supply to +3.3V and turn it off. Connect the positive lead to V<sub>CC</sub> post and the negative lead to GND post.
8. Connect the /EN input to the GND to enable the DOUT and /DOUT output buffers.
9. Connect a DMM or similar voltage measurement device between the LOS<sub>LVL</sub> pin and V<sub>CC</sub>.
10. Connect a second DMM or similar voltage measurement device between the LOS output and GND. For the remainder of this document this DMM will be referred to as the LOS DMM.
11. Connect the pattern generator with differential outputs as a data source to the DIN and /DIN inputs on the SY84403BL evaluation board. Use matched length differential cables.
12. Turn the power supply on.
13. Adjust the trimpot R1 so the voltage at the LOS<sub>LVL</sub> pin is around 1.3V below V<sub>CC</sub>. This sets the LOS for maximum sensitivity. At this level the LOS output should go HIGH or LOW (measured with the LOS DMM set up in step 4) as the input voltage swing at DIN and /DIN is varied around 5mV<sub>PP</sub>.
14. Now adjust the trimpot is to vary the voltage so it is closer to V<sub>CC</sub>. Note that as the voltage at the LOS<sub>LVL</sub> pin approaches V<sub>CC</sub> a larger input voltage swing is required to trigger the assert and deassert levels.
15. The hysteresis between the assert and de-assert levels can be calculated with the following equation:

Hysteresis (dB) = 20log (LOS de-assert voltage/LOS assert voltage). This hysteresis should be >2dB.

## Evaluation Board Layout

The evaluation boards are constructed with Rogers 4003 material and are coplanar in design, fabricated to minimize noise, achieve high bandwidth and minimize crosstalk.

L1	GND and Signal
L2	GND
L3	VCC
L4	GND

Table 1. Layer Stack

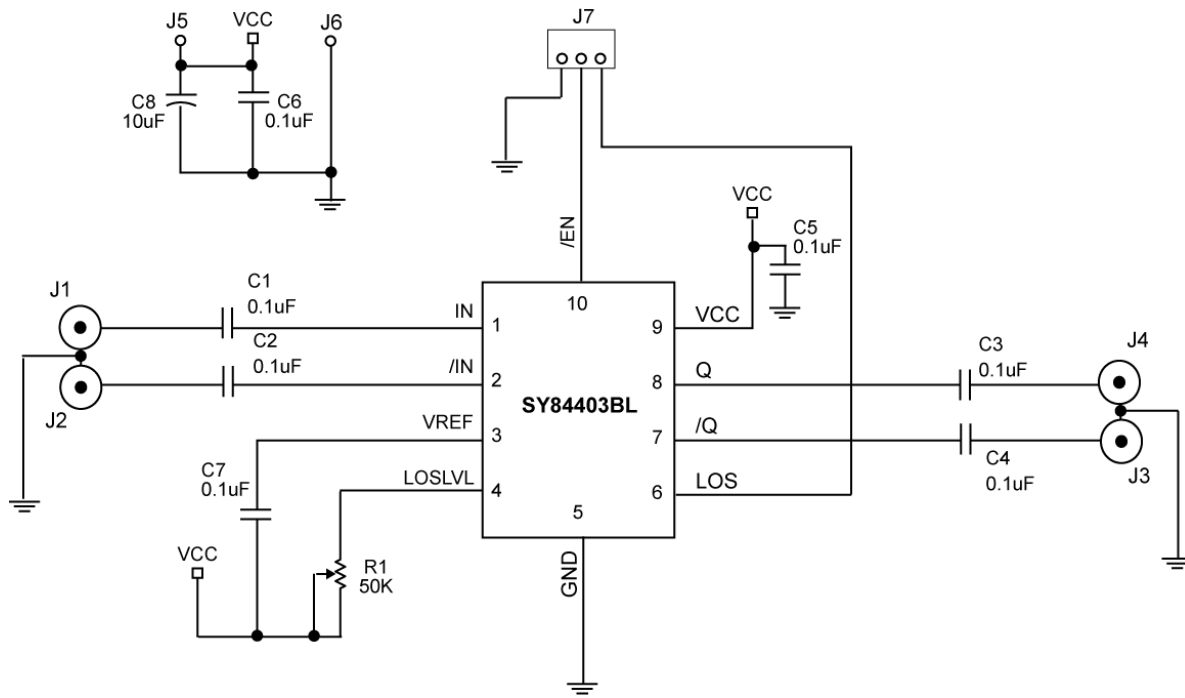


Figure 1. Evaluation Board Schematic

**Bill of Materials (SOIC)**

Item	Part Number	Manufacturer	Description	Qty.
C1-C7	VJ0402Y104KXXAT	Vishay <sup>(1)</sup>	0.1 $\mu$ F, 25V, 10% Ceramic Capacitor, Size 0402, X5R, Dielectric	7
C8	293D105X0025CT	Vishay <sup>(1)</sup>	1 $\mu$ F, Surface Mount Capacitor, Size C	1
R1	3269W-1-153G	Bourns <sup>(2)</sup>	50k $\Omega$ Trimpot	1
J1-J4	142-0701-851	Johnson Components <sup>(3)</sup>	Jack Assembly End Launch SMA	4
U1	<b>SY84403BL</b>	<b>Micrel, Inc.</b> <sup>(4)</sup>	<b>Post Amplifier</b>	1

**Notes:**

1. Vishay: [www.vishay.com](http://www.vishay.com).
2. Bourns: [www.bourns.com](http://www.bourns.com).
3. Johnson Components: [www.johnsoncomponents.com](http://www.johnsoncomponents.com).
4. **Micrel, Inc.:** [www.micrel.com](http://www.micrel.com).

## HBW Support

Hotline: 408-955-1690

Email Support: [HBWHelp@micrel.com](mailto:HBWHelp@micrel.com)

## Application Hints and Notes

For application notes on high-speed termination on PECL and LVPECL products, clock synthesizer products, SONET jitter measurement, and other High Bandwidth product, go to Micrel's website at <http://www.micrel.com/>. Once in Micrel's website, follow the steps below:

1. Click on "Product Info."
2. In the Applications Information Box, choose "Application Hints and Application Notes."

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**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**  
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

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