

FEATURES

- Single 3.3V power supply
- AC-coupled differential inputs
- Simple switch and jumper configuration
- Both CML and PECL signal outputs available

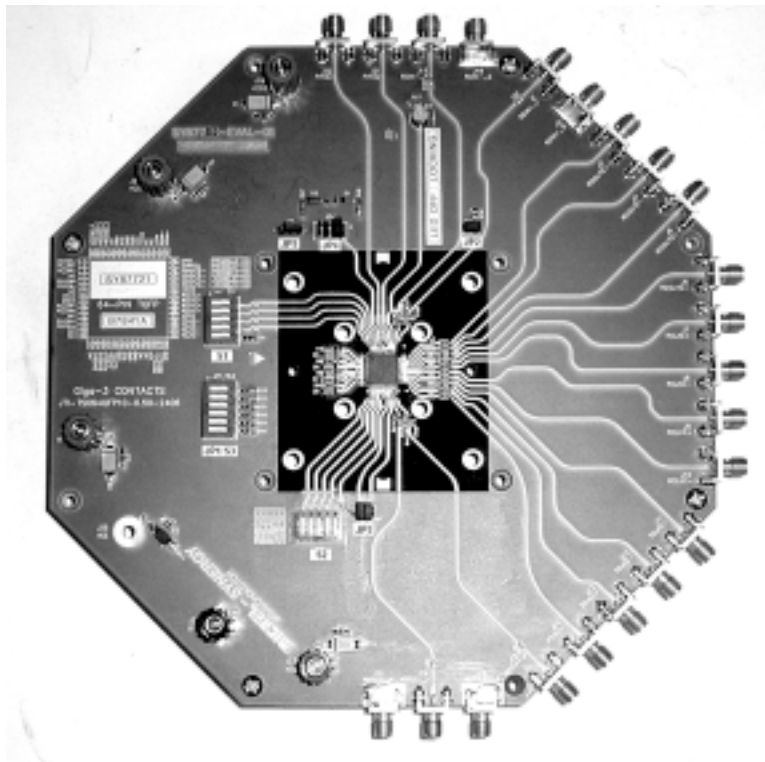
DESCRIPTION

The SY87721L Clock and Data Recovery (CDR) chip is a high-performance IC that is designed to provide protocol-independent clock and data recovery at any data rate between 28Mbps and 2.7Gbps. It is compliant with Bellcore, ITU/CCITT, and ANSI specifications for applications such as SONET, ATM, FDDI, Gigabit Ethernet, Fibre Channel, SMPTE292, and HDTV.

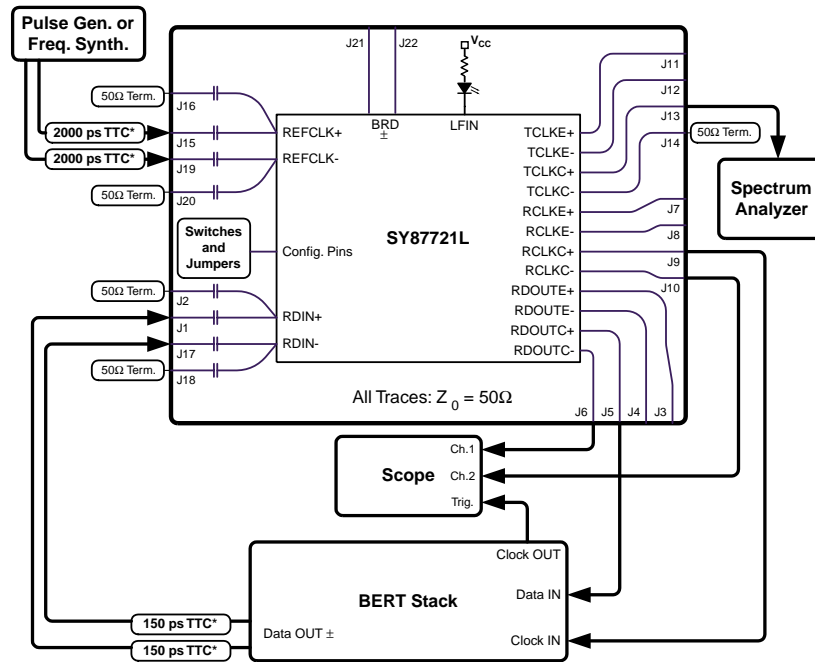
This document provides design and implementation information, as well as a detailed description of the SY87721L evaluation board.

The evaluation board is intended to provide a convenient test and evaluation platform for the SY87721L Clock and Data Recovery (CDR) device. This board can be used for many types of jitter tests, including SONET compliance of the SY87721L, as well as PLL characterization.

EVALUATION BOARD



FUNCTIONAL BLOCK DIAGRAM



*Note: TTC = HP / Agilent Transition Time Converter.
 150ps: HP15435A
 2000ps: HP15438A
 This example uses the CML outputs.
 To use PECL outputs, remove JP2 and connect to PECL outputs.

Figure 1. SY87721L Evaluation Board and Test Setup

FUNCTIONAL DESCRIPTION

The evaluation board simplifies test and measurement of the SY87721L by allowing easy setting of the configuration pins, and convenient connection to all of the SY87721's inputs and outputs. This section covers the various parts of the SY87721L evaluation board, and includes detailed information about these blocks. Performance of the SY87721L can be easily evaluated by following the step-by-step instructions found in the "Test Configuration" section.

Power Supply

The SY87721L is a 3.3V device. Therefore, V_{CC} , V_{CCO} , and V_{CCA} should all be connected to +3.3V, and GND connected to 0V. V_{EE} (J25) is not used. Consult the "Evaluation Board Schematic" section of the SY87721L data sheet for a drawing of the recommended power supply connections.

Board Design and Layout

The evaluation board is a high quality 8-layer design that is meticulously designed to achieve high bandwidth, minimal noise, and minimal crosstalk.

This board uses a "Force-Sense" design on the signal inputs where the signal pin on the SY87721L is located on a 50 Ω transmission line midway between the Force ("_F") and Sense ("_S") SMA connectors. This is handy for monitoring inputs to the SY87721L (such as input jitter). However, a 50 Ω terminator needs to be put on all unused sense outputs unless you are connecting an instrument to monitor that input.

Jumpers, Switches, and LEDs

The SY87721L Evaluation Board features one LED for monitoring the Link Fault Indicator (LFIN) pin. When the LED is on, the data recovery PLL is not locked.

There are three switch blocks. JP1/S3 is not used and should be set to OPEN (1).

Signal Inputs

All signal inputs on this evaluation board are 3.3V PECL and are AC coupled. Therefore, it is sufficient to set the input amplitude to 800 mV_{PP} with no DC offset.

If you are using a high frequency clock or pulse generator (such as the Agilent 8133) to drive REFCLK, you will need to insert a 2000 ps Transition Time Converter (TTC) to slow its edges down.

If you are using a high frequency bit error rate tester (such as the Agilent 70843B Error Performance Analyzer) to drive RDIN \pm , you will need to insert a 150 psec Transition Time Converter (TTC) to slow its edges down. For data rates < 1 Gb/sec, a 250 psec TTC is fine.

Signal Outputs

The SY87721L features both CML and PECL outputs. However, they cannot be used simultaneously. To use the CML outputs, place a jumper on JP2. To use PECL, remove JP2. The PECL outputs are 100k compatible and are temperature compensated. Refer to schematic on page 12.

The CML output voltage swing is controlled by JP3. For normal operation (400mV to 800mV swing), there should be two jumpers arranged in a side-by-side in the same orientation as switch block S2. For reduced CML output swing, remove both jumpers on JP3.

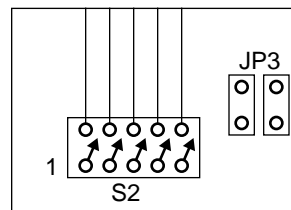


Figure 2. JP3 Configuration for Full CML Output Swing

The BRD \pm outputs (J21 and J22) are CML only.

Performance Considerations

The REFCLK Multiplier selected affects the jitter monitored on the outputs. Larger REFCLK multipliers correspond to higher output jitter. The reason for this is that the phase detector receives fewer edges to update the VCO frequency. The REFCLK multiplier is controlled by the DIVSEL1-3 settings on the S2 jumper block. Lower values of DIVSEL correspond to lower REFCLK multipliers, and lower jitter generation.

This section contains step-by-step instructions for configuring the SY87721L for recovering the clock and data from the data stream of a BERT stack.

1. Set all switches on JP1/S3 jumper block to Open (Off).
2. Set switches on demo board for desired data and clock frequencies.

There are eight switches in Switch Blocks 1 and 2: VCOSEL1-2, FREQSEL1-3, and DIVSEL1-3.

Refer to Appendix A to determine the correct switch settings.

3. Set ENPECL jumper:
Remove jumper on JP2 if PECL output is desired.
Place jumper on JP2 if CML output is desired.
4. Set CD jumper:
Place jumper on rightmost pair (closest to dot) on JP4.
Ensure that there are no other jumpers on JP4.
5. Set ALRSEL (Auto Lock Range) Switch (S2-4):
Set to 1 (HIGH). Refer to "AC Electrical Characteristics" in data sheet for more info.
6. Set BRDMX (BRD Mux) to desired setting.
Place jumper on 1-2 (+ side) of JP5 to have RDOU signal on BRD \pm (J21 & J22).
Place jumper on 2-3 (- side) of JP5 to have RDIN signal on BRD \pm (J21 & J22).

TEST CONFIGURATION

- (Ensure that a jumper is on either 1-2 or 2-3, even if BRD± is unused.)
7. Set CLKSEL switch (Switch 2-5) to 0 so that the frequency synthesizer output appears on TCLK.
 8. Connect the GND connector to power supply ground.
 9. Connect a single +3.3V supply to all four red V_{CC} connectors, and apply power.
 10. Connect REFCLK inputs to reference clock.

Single-ended clock input: Connect REFCLK+_F to clock signal generator, and put 50Ω terminators on REFCLK+_S, REFCLK-_S, and REFCLK-_F.

Differential REFCLK input: Connect the REFCLK±_F inputs to the test equipment and put 50Ω terminators on both REFCLK+_S and REFCLK-_S.

REFCLK is an AC-coupled PECL input whose amplitude swing is 700 mV.

**IMPORTANT:* If using Agilent 8133A Pulse Generator (or other high bandwidth clock source), use 150ps Time Transition Converters on the 8133 outputs.
 11. Connect TCLK outputs to data inputs on test equipment.

There are two sets of data outputs: CML and PECL.

If using PECL: Connect the TCLKE± inputs to DATA IN on test equipment

If using CML: Connect the TCLKC± inputs to DATA IN on test equipment.

** If single-ended TCLK will be used, connect the (+) leg to data input, and put a 50Ω terminator on the unused (-) output.*
 12. Monitor TCLK outputs to ensure that the expected clock is present.

For instance, if DIVSEL is 4, and input clock is 155 MHz., then a 622 MHz. clock should be present on TCLK.

Quick check: Verify that the current draw with the reference clock applied and no data on RDIN is approximately 400 mA.

After checking this, TCLK can be disconnected from the scope and 50Ω terminators can be put on TCLK outputs.
 13. Set CLKSEL switch to select what appears on TCLK outputs:

(This step is necessary only if TCLK output will be used.)

Set Switch 2-5 to 1 for the CDR recovered clock.

Set Switch 2-5 to 0 for frequency synthesizer output.
 14. Connect RDIN inputs to data source.

Connect the RDIN± inputs to DATA OUT on test equipment and put 50Ω terminators on RDIN+_S and RDIN-_S.

RDIN is an AC-coupled PECL input whose amplitude swing is 700mV.

** If single-ended RDIN will be used, connect RDIN+_F to data source, and put 50Ω terminators on RDIN+_S and RDIN-_S*
 15. Connect RDOOUT outputs to data inputs on test equipment.

There are two sets of data outputs: CML and PECL.

If using PECL: Connect the RDOUTE± inputs to DATA IN on test equipment

If using CML: Connect the RDOUTC± inputs to DATA IN on test equipment.

** If single-ended RDOOUT will be used, connect the (+) leg to data input, and put a 50Ω terminator on the unused (-) output.*
 16. Connect RCLK outputs to clock inputs on test equipment.

There are two sets of recovered clock outputs: CML and PECL.

If using PECL: Connect the RCLKE± inputs to DATA IN on test equipment

If using CML: Connect the RCLKC± inputs to DATA IN on test equipment.

** If single-ended RCLK will be used, connect the (+) leg to data input, and put a 50Ω terminator on the unused (-) output.*
- Note:** Upon completion of these steps, the Link Fault LED should go out, indicating that the receive PLL has locked to incoming data.

FREQUENTLY ASKED QUESTIONS

What Do I Do with the Exposed Pad on the Bottom of the Package?

The purpose of the exposed pad at the bottom of the package is to conduct heat more efficiently out of the package. Create a matrix of vias to V_{EE} immediately underneath the exposed pad and solder the vias to the pad. Although the pad is connected to ground, there has not been any degradation in either output generated jitter or input jitter tolerance performance.

I Just Got my Evaluation Board and I Cannot Get Anything to Work.

First check the power supplies. This evaluation board uses one power supply. You should see a current draw of about 0.5 amp when the part is running normally. After that, check voltage swing levels of REFCLK. It is important to focus on getting the synthesizer (CMU) to work first (REFCLK to TCLK), before the data recovery side. TCLK synthesizer sets up the coarse adjust for the VCO in the CDR (or CRU), so if TCLK is not oscillating at the right frequency, the CDR will not lock. Another tip, use a frequency counter like HP53132A to measure frequency of TCLK - it is often more foolproof than using the DSO. If using a DSO scope, like the Agilent CSA803, or the 11801 from Tektronix, trigger off of the REFCLK clock source.

After the synthesizer is operating as expected, make sure to change the trigger on the oscilloscope to trigger on the data generation instrument, such as second HP8133A, a Microwave Logic 1400, or HP70004A,70841 BERT stack. The BERT stack has a "clock output", that be used to trigger the scope. The instrument generating REFCLK is not phase/frequency locked to the data generation side, so it would be impossible to examine an "eye" diagram.

Check the eye of the output source directly first, before going into the device. Most data generation instruments have deskew capability. It is important to deskew both the instrument and the \pm coaxial cables into the DSO, otherwise you'll have too much apparent deterministic jitter.

Aside from setting the VCOSEL, DIVSEL, and FREQSEL incorrectly, everything should operate as expected at this point.

Should I AC or DC Couple the PECL Inputs and Outputs on My Own Board Design?

It is much more difficult to maintain high signal integrity with AC coupling when approaching 2Gbps. If possible, use only microstrip or stripline DC traces. If you AC couple, make the coupling capacitors consistent with the trace width and verify board design using TDR techniques.

What's TDR?

TDR stands for Time Domain Reflectometry, and is used to verify impedance continuity along a signal path. Many interconnects, such as SMA, if not launched correctly onto the PCB will exhibit inductive like resonance with an abrupt capacitive discontinuity. This discontinuity will subtract signal from the inputs and outputs and effectively close the resulting data eye.

What Should I Use to Generate REFCLK in My Design?

This depends on data rate, jitter budget, and cost. However, REFCLK input jitter will affect the overall jitter performance of the system. A fundamental tone crystal-based oscillator is ideal. Measure the jitter of the oscillator with a Wavecrest DTS2077 or a CSA803. A measurement above the 3 psec noise floor of the instrument is too high. Remember that the REFCLK input is multiplied by the DIVSEL selected value, so the resulting jitter increases by $20\log$ (divide ratio). If you use a clock derived from an ASIC, verify the single cycle and accumulated cycle jitter.

Crystal based oscillators typically have poor AC power supply rejection ratio, and if you are providing board power via 400kHz switching supplies you may have to provide some level of filtering, not just bypassing, for the supplies. Also verify that the oscillator output has no "pedestals" in the response due to improper impedance matching and/or inadequate drive capability of the oscillator.

Do not use CMOS based PLLs. They almost always have too much high frequency deterministic jitter for this application. Also fanning out one oscillator to several locations on your board is not a good idea. Crosstalk and inadequate drive can adversely affect performance. We recommend Raltron, Mutron, CTS, Plantronics, Frequency Management, etc., as vendors of crystal-based fundamental tone oscillators.

Can you Suggest a Bypass/Decoupling Scheme?

The SY87721L data sheet contains the evaluation board schematic, and a bill of materials list is included in this document. We have found this arrangement to be an excellent starting point. In addition, most system designs could be dramatically improved by spacing the power planes between ground planes to lower the self-inductance of the power distribution.

FREQUENTLY ASKED QUESTIONS

What Layout Tips Do You Have?

1. Establish controlled impedance stripline, microstrip, or co-planar construction techniques for high-speed signal paths.
2. All differential paths are critical timing paths, and skew should be matched to within ± 10 psec.
3. Signal trace impedance should not vary more than $\pm 5\%$. If in doubt, perform TDR analysis of signal traces.
4. Maintain compact filter networks as close to filter pins as possible.
5. Provide ground plane relief under filter path to reduce stray capacitance and be careful of crosstalk coupling into the filter network.
6. Maintain low jitter on the REFCLK input by isolating the crystal oscillator from power supply noise by adequately decoupling.
7. Keep crystal oscillator close to SY87721L.
8. High speed operation may require use of fundamental-tone crystal based oscillator for optimum performance. (Third overtone oscillators typically have more jitter.)
9. Isolate the input, output, and REFCLK signal traces from other clock and data signals on your board if these other traces are within 3x the trace width. Isolation can be achieved by putting ground traces in between.

Should I Adjust the Loop Filter?

The values found in the data sheets are the result of extensive modeling as well as lab testing. Therefore, we recommend starting with those values. We are presently working on some tools for our customers to use to assist in predicting loop response for given RC filter values. Selecting values to simply reduce jitter does not work since there is a trade-off in jitter generation and jitter tolerance. However, for telecom applications under Bellcore/ITU/CCIT specifications it may be advantageous to adjust the values to trade off jitter transfer for jitter generation.

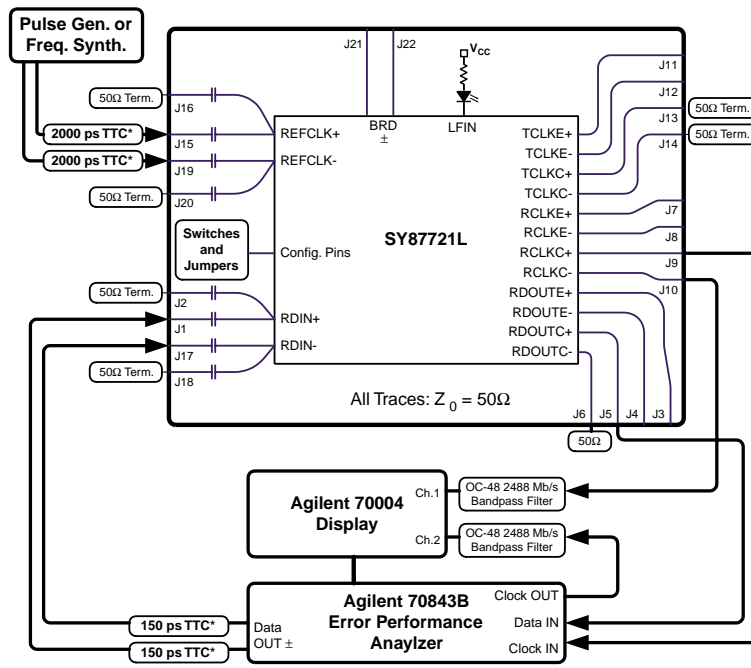
How Do You Suggest We Qualify and Evaluate Performance?

Evaluation should start by measuring the jitter of the REFCLK input. The Clock Multiplier Unit (CMU) is simply a PLL. It multiplies the incoming REFCLK frequency, and jitter will usually worsen. The HP8133A pulse generator is ideal, and the user should include a Transition Time Converter on the 8133s output to slow its edges down. Make sure the rise/fall times are reasonable (not 28 psec rise/fall found on the 12 Gb/s HP BERT clocks!) and 150 psec TTCs will ensure this. Measure the TCLK output jitter using either the \pm side, with the other side terminated. Suitable instruments for measuring the TCLK jitter are the CSA803, 11801, or the Wavecrest 2077. See Figure 1 for descriptions of set up. Characterization of the jitter must include accumulation of many cycles or periods down to a specified low pass corner frequency. The Wavecrest instrument makes this easy with their 6.1 Version software since the user can specify a low pass corner for the collected jitter. The Wavecrest instrument cannot be set up for single period measurements, but must look at the difference between the rising edges of the REFCLK and the TCLK using both channels and performing a histogram of the propagation time between the input REFCLK (which is the HP8133A trigger divided by 1) and the output TCLK. This analysis is very similar to examining a communication channel using a low jitter recovered clock as described in Method of Jitter Specification t11.2 Document.

Evaluation of the CDR is similar, except that the RCLK and RDOUT outputs are used instead. The procedure for measuring the RCLK jitter is identical to the above procedure for TCLK jitter.

Evaluation of the output jitter on RDOUT using RCLK as a trigger source isn't trivial, as the minimum time between the scope trigger and measurement is 24 ns for the Agilent 86100A scope. Therefore the user must delay the data by the same amount, so that the jitter on RDOUT is measured with respect to the correct clock edge. This is important, as the SY87721L will retiming the edges on RDOUT so that they better align with RCLK. The Wavecrest DTS2077 can also be used.

The setup for SONET jitter compliance tests is shown in Figure 2. Agilent provides software for automated Bellcore jitter compliance tests. Contact Agilent for details.



*Note: TTC = HP / Agilent Transition Time Converter.
This example uses the CML outputs.
To use PECL outputs, remove JP2 and connect to PECL outputs.

Figure 2. Equipment Set-up for SONET-OC-48 Jitter Compliance Tests

JUMPERS AND SWITCH BLOCKS

Jumpers/ Switches	Pin Names	Function	Description
JP1	Reserved	Open (1)* Closed (0)	Normal operation. Not used.
JP2	ENPECL (TTL)	Open (1) Closed (0)*	PECL outputs selected, CML outputs disabled. CML outputs selected, PECL outputs disabled.
JP3	CMLSET1,2	Open Closed*	CML output voltage swing of 200mV to 400mV, depending on load. CML output voltage swing of 400mV to 800mV, depending on load.
JP4	CD (PECL)	1-2* (next to dot) 3-4 (middle block) 5-6 (away from dot)	HIGH ($V_{CC}-0.95V$); Normal Operation LOW ($V_{CC}-1.65V$); Clock Recover Disabled (Fault detected) CD tied to V_{CC} ; Do not use.
JP5	BRDMX (TTL)	1-2 (high) 2-3* (low)	RDOUT_C \pm appear on BRD \pm pins (J21 & J22) RDIN \pm appear on BRD \pm pins (J21&J22)
Switch 1			
S1-1, 2, 3	FREQSEL (TTL)		Output clock frequency select.
S2-4, 5	VCOSSEL (TTL)		Output clock frequency range select.
Switch 2			
S2-1, 2, 3	DIVSEL (TTL)		Frequency divider select.
S2-4	ALRSEL (TTL)	Open (0) Closed (1)*	4500 ppm frequency error for "out-of-lock" condition. 500 ppm frequency error for "out-of-lock" condition. (default)
S2-5	CLKSEL (TTL)	Open (0) Closed (1)*	Frequency synthesizer appears on TCLK. Recovered clock appears on TCLK (normal operation)
Switch 3			
S3-1-6	Reserved		Must be set to Open (1).

* = default

DESCRIPTION OF CONNECTORS

Connector	Name	Type	Connects to	Description
J1	RDIN+_F	PECL	RDIN+ (Pin 49) (AC-coup.) RDIN+_S	Read Data In (Force)
J2*	RDIN+_S	PECL	RDIN+ (Pin 49) (AC-coup.) RDIN+_F	Read Data In (Sense)
J3	RDOUTE+	PECL	RDOUTE+ (Pin 46)	Diff. PECL Read Data Out
J4	RDOUTE-	PECL	RDOUTE- (Pin 45)	Diff. PECL Read Data Out
J5	RDOUTC+	CML	RDOUTC+ (Pin 44)	Diff. CML Read Data Out
J6	RDOUTC-	CML	RDOUTC- (Pin 43)	Diff. CML Read Data Out
J7	RCLKE+	PECL	RCLKE+ (Pin 41)	Diff. PECL Recovered Clock
J8	RCLKE-	PECL	RCLKE- (Pin 40)	Diff. PECL Recovered Clock
J9	RCLKC+	CML	RCLKC+ (Pin 39)	Diff. CML Recovered Clock
J10	RCLKC-	CML	RCLKC- (Pin 38)	Diff. CML Recovered Clock
J11	TCLKE+	PECL	TCLKE+ (Pin 36)	Diff. PECL Transmit Clock
J12	TCLKE-	PECL	TCLKE- (Pin 35)	Diff. PECL Transmit Clock
J13	TCLKC+	CML	TCLKC+ (Pin 34)	Diff. CML Transmit Clock
J14	TCLKC-	CML	TCLKC- (Pin 33)	Diff. CML Transmit Clock
J15	REFCLK+_F	PECL	REFCLK+ (Pin 31) (AC-coup.) REFCLK+_S	Reference Clock In (Force)
J16*	REFCLK+_S	PECL	REFCLK+ (Pin 31) (AC-coup.) REFCLK+_F	Reference Clock In (Sense)
J17	RDIN-_F	PECL	RDIN- (Pin 50) (AC-coup.) RDIN-_S	Read Data In (Force)
J18*	RDIN-_S	PECL	RDIN- (Pin 50) (AC-coup.) RDIN-_F	Read Data In (Sense)
J19	REFCLK-_F	PECL	REFCLK- (Pin 30) (AC-coup.) REFCLK-_S	Reference Clock In (Force)
J20*	REFCLK-_S	PECL	REFCLK+ (Pin 30) (AC-coup.) REFCLK-_F	Reference Clock In (Sense)
J21	PIN52	CML	BRD+ (Pin 52)	Buffered Recovered Data (output depends on BRDMX)
J22	PIN53	CML	BRD- (Pin 53)	Buffered Recovered Data (output depends on BRDMX)
J23	VCC	Power		
J24	GND	Ground	Ground Plane	Ground
J25	VEE	Ground	Ground (AC-coupled config.)	-1.3V (DC-coupled config.)
J26	VCCA	Power	Pin 8 (after filtering)	Power for Analog Circuits
J27	VCC	Power	VCC Power Pins (after filtering)	Power for Digital Circuits
J28	VCCO	Power	Pins 37, 42, 54 (after filtering)	Power for Output Drivers

* Place 50Ω SMA termination plug on this connector if it isn't used for monitoring that input.

ALL POSSIBLE LEGAL FREQUENCY AND DIVIDER SELECTIONS

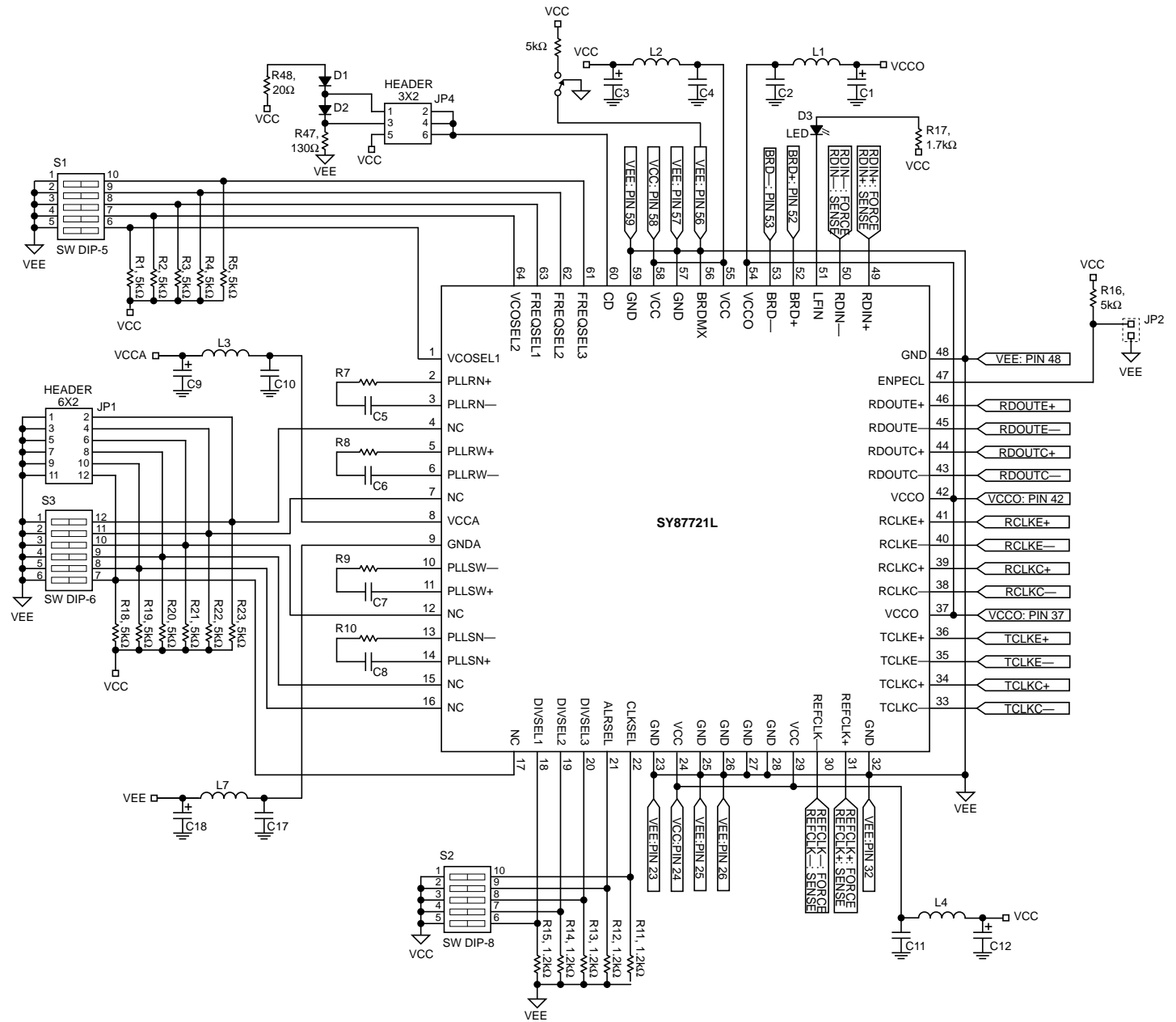
The selections in gray are the specific selections to be used to verify the evaluation board.

VCO Sel1	VCO sel2	Freq sel1	Freq sel2	Freq sel3	Div sel1	Div sel2	Div sel3	VCO Mbps	Div	Low Ref Clk	Hi Ref Clk		
0	0	0	0	0	1	0	0	2488.32*	8	311		OC-48 16-bit	
					1	0	1		10	248.8			
					1	1	0		16	155.52			
					1	1	1		20	124.4			
					0	1	1		32	77.76			
		0	0	1	0	1	0	0	1244.166	4	311		OC-24
		1	0	0	8	155.52							
		1	0	1	10	124.4							
		1	1	0	16	77.76							
		1	1	1	20	62.2							
	0	1	0	0	0	0	1	622.08	2	311		OC-12 8-bit	
	0	1	0	4	155.52								
	1	0	0	8	77.76								
	1	0	1	10	62.2								
	1	1	0	16	38.88								
	1	1	1	20	31.1								
	1	0	0	0	0	0	0	0	311.04	1	311		OC-6
						0	0	1		2	155.52		
						0	1	0		4	77.76		
						1	0	0		8	38.88		
1						0	1	10		31.1			
1		1	0	16	19.44								
1		1	1	20	15.552								
1		1	0	0	0	0	0	155.52	1	155.52		OC-3 8-bit 4-bit	
0		0	1	2	77.76								
0		1	0	4	38.88								
1	0	0	8	19.44									
1	0	1	10	15.552									
1	1	0	16	9.72									
1	1	1	20	7.776									
0	1	0	0	0	1	0	0	1800-2500*	8	225	312.5		
					1	0	1		10	180	250		
					1	1	0		16	112.5	156.25		
					1	1	1		20	90	125		
					0	1	1		32	56.25	78.125		
1	0	0	0	0	0	1	0	1250-1800	4	312.5	450		
					1	0	0		8	156.25	225		
					1	0	1		10	125	180		
					1	1	0		16	78.125	112.5		
					1	1	1		20	62.5	90		
					0	1	1		32	39.06	56.25		
1	1	0	0	0	0	1	0	625-1250	4	156.25	312.5	FC 10-bit 20-bit	
					1	0	0		8	78.125	156.25		
					1	0	1		10	62.5	125		
					1	1	0		16	39.0625	78.125		
					1	1	1		20	31.25	62.5		
					0	1	1		32	19.53125	39.06		

* If the Gigabert 1400 is used, then only the Transmit VCO can be verified above 1.25GHz. To verify both the Transmit and Receive above 1.25GHz, the HP BERT must be used. As an alternative, the Receive VCO can be verified for lock by monitoring the recovered Clock & Data with the HP11801B Scope.

VCO Sel1	VCO sel2	Freq sel1	Freq sel2	Freq sel3	Div sel1	Div sel2	Div sel3	VCO Mbps	Div	Low Ref Clk	Hi Ref Clkf						
		0	0	1	0	0	1	325-650	2	162.5	325	FC/2					
					0	1	0		4	81.25	162.5						
					1	0	0		8	40.625	81.25						
					1	0	1		10	32.5	65						
					1	1	0		16	20.3125	40.625						
					1	1	1		20	16.25	32.5						
					0	0	0		170-340	1	170		340				
		0	0	1	2	85	170										
		0	1	0	4	42.5	85										
		1	0	0	8	21.25	42.5										
		1	0	1	10	17	34										
		1	1	0	16	10.625	21.25										
		1	1	1	20	8.5	17										
		0	1	1	1	0	0	0	0	109-208	1	109	208				
											0	0	1		2	54.5	104
											0	1	0		4	27.25	52
											1	0	0		8	13.625	26
											1	0	1		10	10.9	20.8
											1	1	0		16	6.8125	13
											1	1	1		20	5.45	10.4
		1	0	0	0	0	0	0	0	82-157	1	82	157				
											0	0	1		2	41	78.5
											0	1	0		4	20.5	39.25
											1	0	0		8	10.25	19.625
											1	0	1		10	8.2	15.7
											1	1	0		16	5.125	9.8125
											1	1	1		20	4.1	7.85
		1	0	1	1	0	0	0	0	55-104	1	55	104				
0	0										1	2	27.5		52		
0	1										0	4	13.75		26		
1	0										0	8	6.875		13		
1	0										1	10	5.5		10.4		
1	1										0	16	3.4375		6.5		
1	1										1	20	2.75		5.2		
1	1	0	0	0	0	0	0	41-78	1	41	78						
									0	0	1		2	20.5	39		
									0	1	0		4	10.25	19.5		
									1	0	0		8	5.125	9.75		
									1	0	1		10	4.1	7.8		
									1	1	0		16	2.5625	4.875		
									1	1	1		20	2.05	3.9		
1	1	1	1	0	0	0	0	28-52	1	28	52						
									0	0	1		2	14	26		
									0	1	0		4	7	13		
									1	0	0		8	3.5	6.5		
									1	0	1		10	2.8	5.2		
									1	1	0		16	1.75	3.25		
									1	1	1		20	1.4	2.6		

EVALUATION BOARD SCHEMATIC



NOTES:

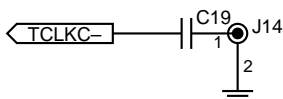
1. C11, C17, C10, C4, C2 = 0.1μF
2. C18, C12, C9, C3, C1 = 1μF
3. C2, C4, C10, C11, and C17 need to be located right at device pin. If vias to power GND used—use overlapping multiple vias to lower inductance.
4. This board can be used with either AC-coupled (default) or DC-coupled inputs.

If inputs are AC-coupled, a ferrite bead replaces C18, and V_{EE} is internally connected to ground.

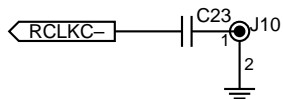
If inputs are DC-coupled, V_{CC} = +2V, V_{CC} = -1.3V. Contact factory for assistance.

EVALUATION BOARD I/O TERMINATION SCHEMES

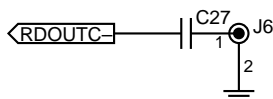
**TCLK
OUTPUTS**



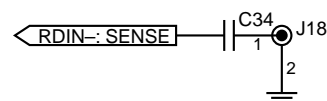
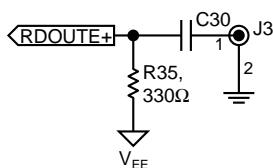
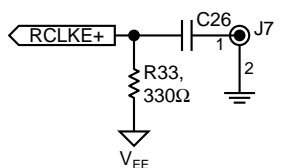
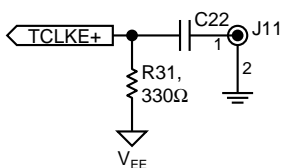
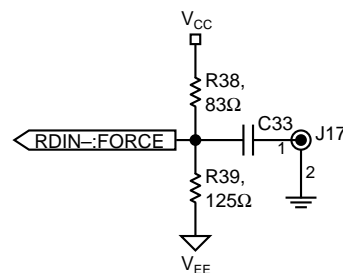
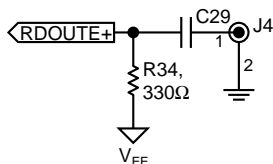
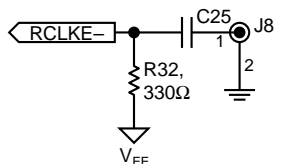
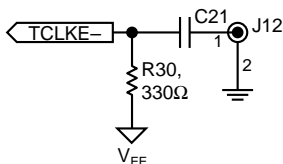
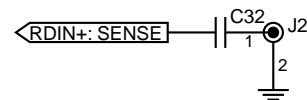
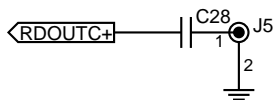
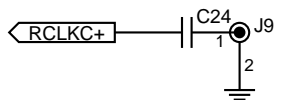
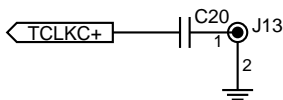
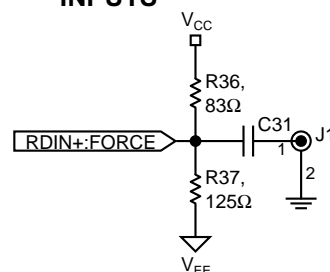
**RCLK
OUTPUTS**



**RDOUT
OUTPUTS**



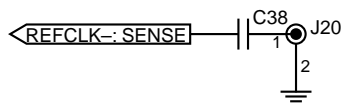
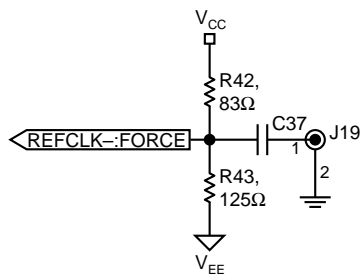
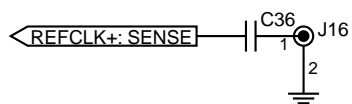
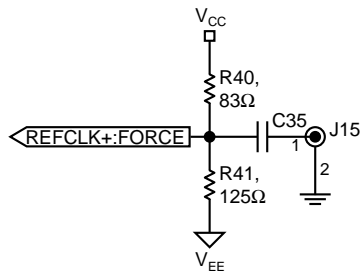
**RDIN
INPUTS**



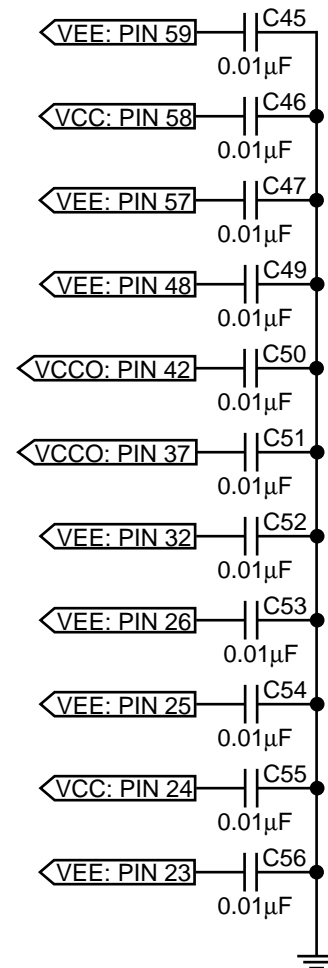
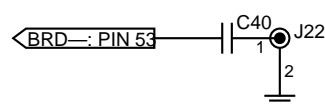
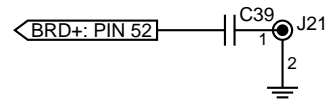
NOTES:

1. For AC-coupling, include capacitors C19 thru C31, C33, C35 and C37.
2. If DC-coupling, remove resistors R36 thru R43.

**REFCLK
INPUTS**



**BRD
OUTPUTS**



BILL OF MATERIALS

Item	Part Number	Manufacturer	Description	Qty.
C1, C3, C9, C12			22 μ F capacitor, size D	4
C18	2743019447		Ferrite bead	1
C2, C4, C10, C11, C17, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56			0.01 μ F capacitor, size 0603	17
C5, C6, C7, C8			1.0 μ F capacitor, size 1206	4
C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38,			0.1 μ F capacitor, size 0603	22
C39, C40			Don't Install	
C41, C42, C43, C44		Don't Install	1000pF capacitor, size 0603	4
D2, D1	1N4148		diode, axial leaded	2
D3			light emitting diode, RED	1
JP1			header 6x2, See note below for footprint	1
JP2, JP3			jumper, 100mil centers, 25mil square pin	2
JP4			header 3x2, 100mil centers, 25mil square pin	1
J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16 J17, J18, J19, J20	142-0701-851	Johnson Components	end launch jack receptacle	22
J21, J22				
J23, J26, J27, J28	111-0702-001 Red	Johnson Components	banana jack	4
J25			Don't install	1
J24	111-0703-001 Black	Johnson Components	banana jack	1
L1, L2, L3, L4, L7	BLM21A102F		Ferrite bead, size 0805	5
R1, R2, R3, R4, R5, R16, R18, R19, R20, R21, R22, R23			5k Ω resistor, size 0805	12
R7			390 Ω resistor, size 0603	1
R8			455 Ω resistor, size 0603	1
R9			845 Ω resistor, size 0603	1
R10			1.2k Ω resistor, size 0603	1
R11, R12, R13, R14, R15			1.2k Ω resistor, size 0805	5
R17			1.7k Ω resistor, size 0805	1
R24, R25, R26, R27, R28, R29, R46			100 Ω resistor, size 0603	7
R30, R31, R32, R33, R34, R35,			330 Ω resistor, size 0603	8
R44, R45			Don't install	
R36, R38, R40, R42			83 Ω resistor, size 0603	4
R37, R39, R41, R43			125 Ω resistor, size 0603	4
R47			130 Ω resistor, size 0805	1
R48			20 Ω resistor, size 0805	1
S2, S1			switch, SW DIP-5	2
S3			switch, SW DIP-6	1
U1	SY87721L	Micrel Semiconductor		1
NOT USED: chip direct soldered	JTI-TS064QFP10- 0.50-2406	Johnstech	contractor	

*JP1/S3 combination footprint (see schematic) will consist of 100-mil centers for JP1 and 300-mil centers for S3.

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