

FEATURES

The SY88773V features:

- Multirate up to 3.2Gbps operation
- Wide gain-bandwidth product
- Low-noise 50Ω CML data outputs
- Chatter-free Loss-of-Signal (LOS) output
- Programmable LOS sensitivity
- On-chip input bias for AC-coupled applications
- TTL /EN input
- Wide power supply and temperature operating range

The SY88773V evaluation board features:

- AC-coupled I/O with SMA connectors
- Single potentiometer to set LOS_{LVL}
- SMA or test points available to measure non-critical nodes

AVAILABLE MEASUREMENTS

The SY88773V evaluation board allows the following measurements:

- Frequency performance
- Output eye pattern generation
- Mask testing
- Jitter
- Output rise/fall time
- BER testing
- Hysteresis measurement

EVALUATION BOARD

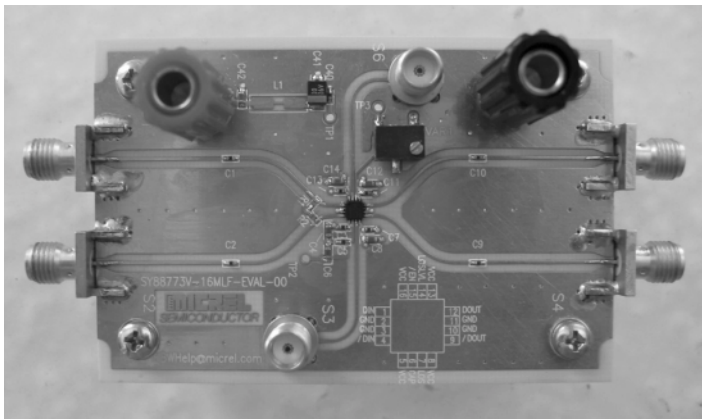


Figure 1. SY88773V Evaluation Board

DESCRIPTION

The SY88773V low-power limiting post amplifier is designed for use in fiber-optic receivers. The device connects to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88773V quantizes these signals and outputs typically 800mV_{pp} voltage-limited waveforms.

The SY88773V operates from a single +3.3V ±10% or +5V ±10% power supply, over an industrial temperature range of -40°C to +85°C. With its wide bandwidth and high gain, signals with data rates up to 3.2Gbps and as small as 10mVp-p can be amplified to drive devices with CML or PECL inputs.

The SY88773V incorporates a loss-of-signal (LOS) open-collector TTL output with internal 5kΩ pull-up resistor. A programmable loss-of-signal level set pin (LOS_{LVL}) sets the sensitivity of the input amplitude detection. LOS asserts high if the input amplitude falls below the threshold set by LOS_{LVL} and deasserts low otherwise. LOS can be fed back to the enable (/EN) input to maintain output stability under a loss of signal condition. /EN deasserts the true output signal without removing the input signal. Typically, 4.6dB LOS hysteresis is provided to prevent chattering.

This manual provides information on the SY88773V evaluation board. It should be used in conjunction with the SY88773V data sheet, which contains full specifications of the SY88773V.

The SY88773V evaluation board enables fast and thorough evaluation of the SY88773V 3.2Gbps CML low-power limiting post amplifier. The board is an easy-to-use, 4-layer high-speed coplanar design. It is designed to be driven by a high-speed 3.2Gbps pattern generator.

The SY88773V evaluation board is intended to be terminated to a 50Ω scope and provides for simple user adjustability of the LOS threshold through the adjustment of an on-board potentiometer. This allows the user to evaluate various parameters of the SY88773V, as listed in the “Available Measurements” section of this document.

Layer	Definition
1	Signal/GND
2	GND
3	VCC
4	GND

Table 1. SY88773V Evaluation Board Layer Stack-Up

MEASUREMENT SETUP

Equipment used for measurements:

1. Agilent 83752A Synthesized Sweeper
2. Agilent 70004A Display
3. Agilent 70843B Error Performance Analyzer
4. Agilent 86100A Wide-Bandwidth Oscilloscope
5. Two (2) MCL BW S15W2 40dB Attenuators
6. Agilent E3620A DC Power Supply
7. Tektronix DMM157 Multimeter
8. Matched High-Speed Cables w/SMA Connectors

Note:

Items 1 through 3 constitute the BERT stack.

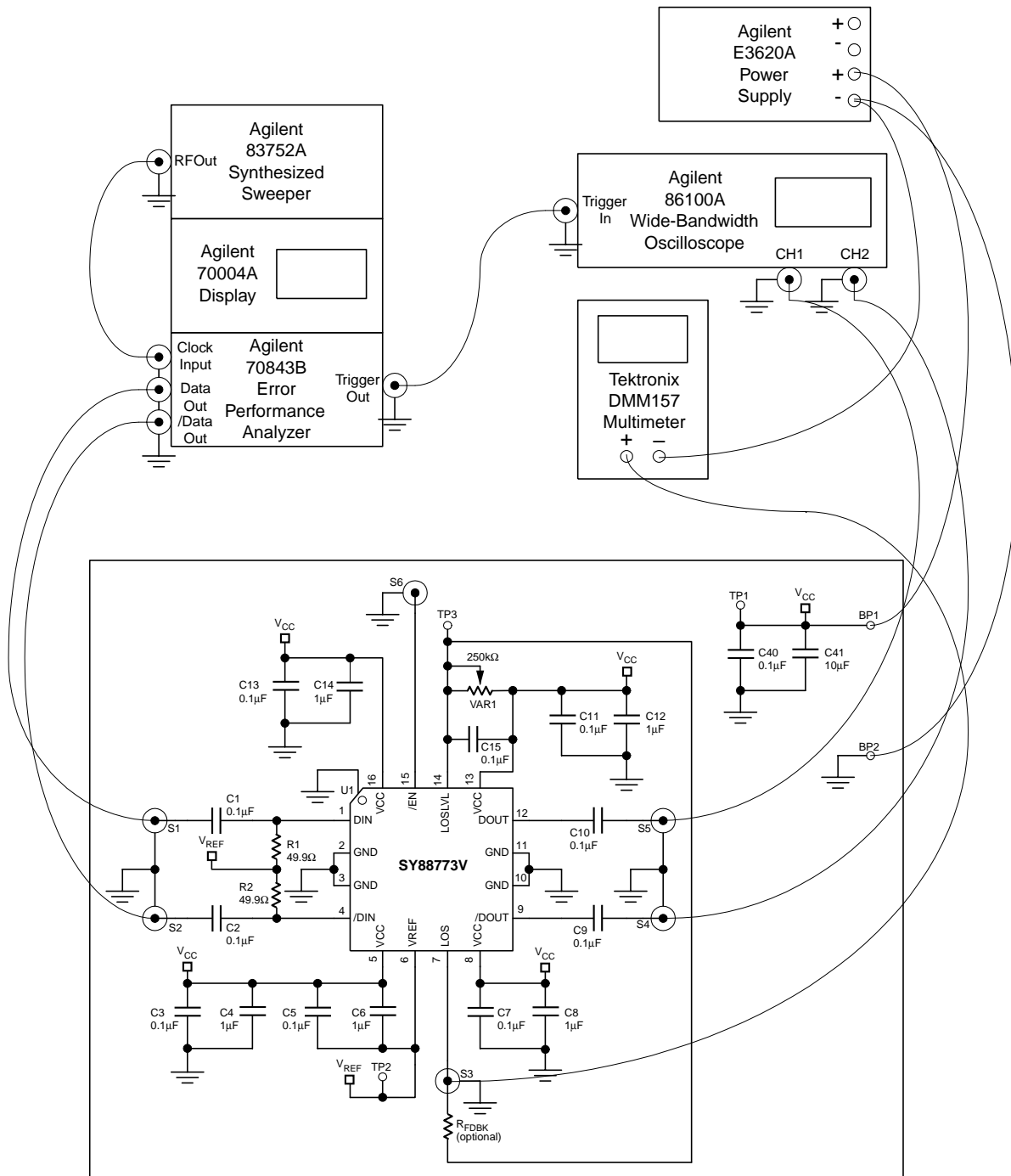


Figure 2. Setup for Measurements

SETUP FOR MEASUREMENTS

This section explains how to connect and setup the SY88773V evaluation board per Figure 2. Ensure proper ESD precautionary measures are taken before handling sensitive electronic equipment, including the SY88773V evaluation board.

1. Set E3620A output to 3.3V and then turn off E3620A. Connect E3620A's positive lead to V_{CC} post, negative lead to GND post.
2. Configure Agilent BERT stack:
 - a. Set the 83752A Synthesized Sweeper to 2.5GHz.
 - b. From the 70004A's Pattern menu, choose the PRBS $2^{31}-1$ pattern.
 - c. From the 70004A's Trigger menu:
 - i. Choose clock as trigger output
 - ii. Choose CLK/8 for divider
 - d. From the 70004A's Data menu:
 - i. External Termination = DC termination 0V
 - ii. Attenuation = 40dB
 - iii. Amplitude = 5mV ($10mV_{pp}$)
 - iv. Hi-Level = 0V
 - v. Tracking = ON
 - vi. Polarity = NORMAL
 - vii. Data Output = ON
 - viii. Crossing = 0
3. Connect 70843V's trigger output to 86100A's trigger input.
4. Short /EN to GND by shorting S6 to GND.
 - a. DOUT will be stuck low if this is not done
5. Connect DIN and /DIN (S1 and S2) on SY88773V evaluation board to 70843V's data outputs through 40dB attenuators.
 - a. Connect 40dB attenuators directly to the board rather than the 70843V's data outputs to allow a larger and cleaner signal to pass through the connecting SMA cables.
6. Connect DOUT and /DOUT (S5 and S4) on SY88773V evaluation board to 86100A's inputs.
7. Set DMM157 to display voltage. Connect positive lead to SD (S3) and connect negative lead to GND.
8. Turn on E3620A. Typical power supply current should be ~45mA. Excessive current usually means the power supply leads have been connected backwards. Be careful of this!
9. Configure 86100A oscilloscope.
 - a. Verify a trigger signal is present by checking that the Trigger Source button is lit.
 - i. Depress this button to choose external source if necessary.
 - ii. Adjust trigger level if necessary.
 - b. Press Eye/Mask Mode on front panel.
 - c. Choose NRZ Eye Measurements from on-screen display.
 - d. Choose RMS Jitter, Rise Time, Fall Time and Eye Amplitude Measurements from on-screen selection list.

MEASUREMENTS

The SY88773V evaluation board assumes the use of a 50Ω scope to terminate the SY88773V. The following sections detail various measurements that the SY88773V evaluation board allows.

1. Eye pattern generation including jitter and rise/fall times:
 - a. Set 70004's Data amplitude to 5mV (10mV_{pp}).
 - b. Press Autoscale on oscilloscope. The eye pattern should automatically display on the scope. If not, verify the steps listed in the "Setup for Measurements" section are completed. Sometimes the waveform needs to be manually adjusted to fit the display. Use the Time Scale and Voltage Scale knobs on the front panel of the scope to adjust this.
 - c. Observe measurements on scope's display. The rise and fall times should be less than 120ps, amplitude around 400mV (800mV_{pp}) and jitter around 10ps_{rms} .
 - i. Note that the output amplitude varies with the input amplitude until the SY88773V enters limiting mode at around 10mV_{pp} input. The SY88773V has a typical gain of 38dB. Hence, 5mV_{pp} input will give only 400mV_{pp} output, whereas $>10\text{mV}_{pp}$ input will give 800mV_{pp} output.

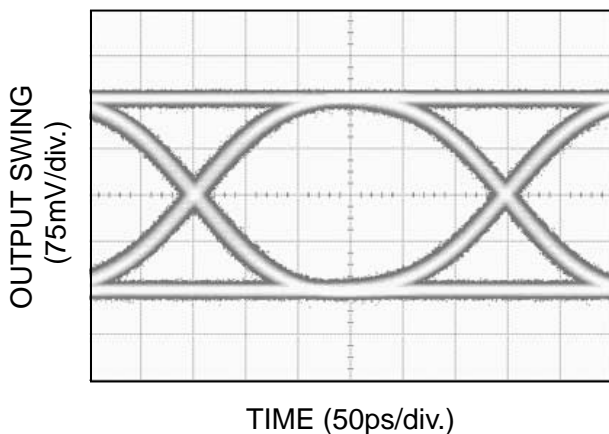


Figure 3. Typical SY88773V Output Eye Pattern from a 10mV_{pp} Input at 3.3V, 25°C

2. Mask testing:
 - a. Press Eye/Mask Mode on front panel of scope.
 - b. Choose Mask Testing from on-screen display.
 - c. Choose Open Mask from on-screen selection list.
 - i. Select and open the OC-48 Mask
 - d. Choose Start Mask Testing from on-screen selection list. Waveform should automatically display with appropriate mask regions and testing will start. If not, verify the steps listed in the "Setup for Measurements" section are completed.
3. BER testing:
 - a. Feedback the SY88773V evaluation board's DOUT output to the 70843V's BERT Data input.
 - b. Feedback the 70843V's Clock output to the 70843V's BERT Clock input.
 - c. Set 70004's Data Amplitude to 5mV (10mV_{pp}).
 - d. From the 70004A's Gating menu:
 - i. Choose a gate condition. The options are: gate by time, errors or bits. Choose bits, but this is of no relevance because there should be no errors, and the test will run forever until manually interrupted if gate by errors is chosen.
 - ii. Choose single gating period.
 - iii. Choose run gating.
 - iv. 70004A will reset error count and synchronize SY88773V's transmitted bitstream to 70843V's generated bitstream. If synchronization does not occur, it is sometimes due to cable length. Try using different length cables to achieve synchronization. If this is unavailable, another trick is to adjust the 83752A's frequency to a slightly higher or lower value.
 - v. At the end of the gating period, there should be no errors.

MEASUREMENTS

4. LOS hysteresis:

The SY88773V evaluation board provides a potentiometer to allow for easy adjustment of LOS_{LVL} without the need for an extra power supply. The potentiometer acts as a variable resistor which is connected from V_{CC} to LOS_{LVL} . The board also contains a provision for a feedback resistor connecting LOS_{LVL} to LOS .

The SY88773V contains an internal $5k\Omega$ pull-up resistor from LOS to V_{CC} . It also contains an internal $2.8k\Omega$ resistor connected from LOS_{LVL} to V_{REF} . V_{REF} is a reference voltage of approximately $V_{CC} - 1.3V$. Hence, LOS_{LVL} can be set to any voltage from V_{CC} to $V_{CC} - 1.3V$, as specified in the SY88773V data sheet. Figure 4 details the configuration between the various pins which set the LOS hysteresis.

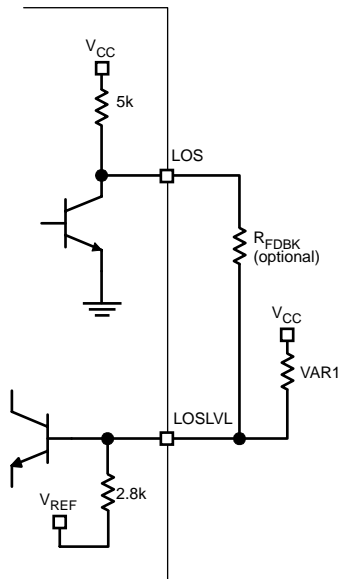


Figure 4. LOS Hysteresis Configuration

From this configuration, LOS_{LVL} will have two different values depending on whether LOS is asserted or deasserted. The feedback resistor causes LOS_{LVL} to be higher when LOS is asserted and lower when LOS is deasserted. In this way, a larger input amplitude is required to deassert LOS than would be required without the feedback resistor. This increased hysteresis and sensitivity are the benefits of the feedback resistor. The equations to

calculate $R_{LOS_{LVL}}$ (the resistance of VAR1) and R_{FDBK} (the feedback resistor connecting LOS_{LVL} to LOS) given V_{CC} , $LOS_{LVL_{LA}}$ and $LOS_{LVL_{LD}}$ are quite cumbersome, but are available in closed form by emailing Micrel's High Bandwidth helpline at hbwhelp@micrel.com. $LOS_{LVL_{LA}}$ is the LOS_{LVL} voltage when LOS asserted and $LOS_{LVL_{LD}}$ is the LOS_{LVL} voltage when LOS is deasserted. $LOS_{LVL_{LA}}$ and $LOS_{LVL_{LD}}$ are chosen for a desired input sensitivity per the LOS assert/deassert vs LOS_{LVL} graph in the SY88773V's data sheet. Note that $LOS_{LVL_{LA}} \geq LOS_{LVL_{LD}}$. Use volts for voltages and $k\Omega$ for resistances in the equations.

If increased hysteresis and sensitivity are not required, the feedback resistor does not need to be installed. Thus there is only one LOS_{LVL} voltage and it can be calculated by the following equation:

$$LOS_{LVL} = V_{CC} - 1.3 \frac{R_{LOS_{LVL}}}{R_{LOS_{LVL}} + 2.8}$$

$R_{LOS_{LVL}}$ is chosen for a desired input sensitivity per the LOS assert/deassert vs $R_{LOS_{LVL}}$ graph in the SY88773V's datasheet. Use volts for voltages and $k\Omega$ for resistances in the equation.

The proceeding steps show how to find the LOS hysteresis for a $10mV_{pp}$ LOS assert voltage without measuring R . Other LOS assert voltages can be used, but the appropriate input signal attenuation is required.

- Set 70004's Data amplitude to $5mV$ ($10mV_{pp}$).
- Verify DMM157 displays that LOS is LOW ($\sim 0.2V$). If not, turn VAR1 until LOS is LOW.
- Turn VAR1 just until LOS is HIGH ($\sim 3.3V$).
- Slowly increase 70004A's Data amplitude until LOS becomes LOW. Note the voltage at which LOS becomes LOW. This is the LOS deassert voltage.
- Now slowly lower the 70004A's Data amplitude until LOS becomes HIGH again. This should be the starting voltage of $5mV$ ($10mV_{pp}$). This is the LOS assert voltage.
- $Hysteresis(dB) = 20\log(LOS \text{ deassert voltage} / LOS \text{ assert voltage})$. This should be $\geq 2dB$.

FREQUENTLY ASKED QUESTIONS

I just got my SY88773V evaluation board and I cannot get anything to work! Where should I start?

First, check the power supplies. Typical power supply current should be ~45mA. Excessive current usually means the power supply leads have been connected backwards. Be careful of this!

If that looks okay, ensure the outputs are enabled by shorting /EN to GND by shorting S6 to GND.

Next, verify the 70004A's Data outputs are enabled and there's sufficient amplitude (at least 10mV_{pp}) to drive the SY88773V.

If the above are okay and there's still nothing displaying on the scope, then there's most likely a trigger setup issue with the scope. Look on the scope's front panel and verify that the instrument is triggered. The Trigger Source button should be lit if a trigger signal is present. If not, press the button until the external trigger is selected. Also, try adjusting the level until a signal is found. If this does not work, verify the 70004A is set to output a CLK/8 trigger signal as described in the "Setup for Measurements" section of this document.

Can you suggest a bypass/decoupling scheme?

Figure 2 shows the power supply decoupling scheme used for the SY88773V evaluation board. The "Bill of Materials" at the end of this document lists the supplier and component values. We have found this arrangement to be an excellent starting point.

What layout tips do you have?

1. Establish controlled impedance stripline, microstrip or coplanar construction techniques for high-speed signal paths.

2. All differential paths are critical timing paths and skew should be matched to within $\pm 10\text{ps}$.

3. Signal trace impedance should not vary more than $\pm 5\%$. If in doubt, perform Time Domain Reflectometry (TDR) analysis of signal traces.

4. Place power supply decoupling capacitors as close as possible to the device's power pins.

What is Time Domain Reflectometry (TDR)?

TDR is used to verify impedance continuity along a signal path. Many interconnects, such as SMA, if not launched correctly onto the PCB, will exhibit inductive-like resonance with an abrupt capacitive discontinuity. This discontinuity will subtract signal from the inputs and outputs, effectively closing the resulting data eye. The 86100A allows TDR testing and is a useful tool to help evaluate your PCB.

I still have questions. Who should I contact?

Micrel's HBW Applications helpline is available to assist you. Please call (408) 955-1690 or e-mail hbwhelp@micrel.com for assistance.

BILL OF MATERIALS

Item	Part Number	Manufacturer	Description	Qty
BP1	111-0702-001	Johnson ⁽¹⁾	red binding post	1
BP2	111-0703-001	Johnson ⁽¹⁾	black binding post	1
C1, C2, C3, C5, C7, C9, C10, C11, C13, C15, C40	PCC1731CT-ND	Panasonic ⁽²⁾	0.1 μ F surface mount capacitor, size 0402	11
C4, C6, C8, C12, C14, C42	PCC1915CT-ND	Panasonic ⁽²⁾	1 μ F surface mount capacitor, size 0603	6
C41	PCC1940CT-ND	Panasonic ⁽²⁾	10 μ F surface mount capacitor, size 1206	1
R1, R2	P49.9LCT-ND	Panasonic ⁽²⁾	49.9 Ω surface mount resistor, size 0402	2
S1, S2, S4, S5	142-0701-851	Johnson ⁽¹⁾	end launch SMA	4
S3, S6	142-0701-201	Johnson ⁽¹⁾	PC mount SMA	2
TP1, TP2, TP3	TSW-101-07-S-S	Samtec ⁽³⁾	0.1mil center through hole terminal strip	2
VAR1	3269W-1-254G	Bourns ⁽⁴⁾	250k Ω potentiometer	1
U1	SY88773V	Micrel, Inc. ⁽⁵⁾	3.2Gbps CML post amplifier	1

Notes:

1. Johnson tel: 800-247-8256
2. Panasonic tel: 800-344-2112
3. Samtec tel: 800-726-8329
4. Bourns tel: 877-426-8767
5. Micrel, Inc. tel: 408-944-0800

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