

## FEATURES

The SY88843V features:

- Multi-rate up to 3.2Gbps operation
- Wide gain-bandwidth product
- Low-noise 50Ω CML data outputs
- Chatter-free Signal Detect (SD) output
- Programmable SD sensitivity
- Internal 50Ω data input termination
- TTL EN input
- Wide power supply and temperature operating range

The SY88843V evaluation board features:

- AC-coupled I/O with SMA connectors
- Single potentiometer to set SDLVL
- SMA or test points available to measure non-critical nodes

## AVAILABLE MEASUREMENTS

- Frequency performance
- Output eye pattern generation
- Mask testing
- Jitter
- Output rise/fall time
- BER testing
- Hysteresis measurement

## EVALUATION BOARD

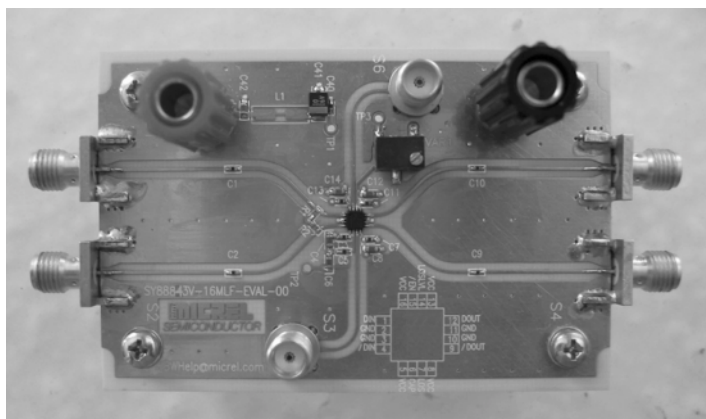


Figure 1. SY88843V Evaluation Board

## DESCRIPTION

The SY88843V low-power, limiting post amplifier is designed for use in fiber optic receivers. The device connects to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88843V quantizes these signals and outputs typically 800mV<sub>pp</sub> voltage-limited waveforms.

The SY88843V operates from a single +3.3V ±10% or +5V ±10% power supply, over an industrial temperature range of -40°C to +85°C. With its wide bandwidth and high gain, signals with data rates up to 3.2Gbps and as small as 10mV<sub>pp</sub> can be amplified to drive devices with CML or PECL inputs.

The SY88843V incorporates a signal detect (SD), open-collector, TTL output with internal 4.75kΩ pull-up resistor. A programmable signal detect level set pin (SD<sub>LVL</sub>) sets the sensitivity of the input amplitude detection. SD asserts high if the input amplitude rises above the threshold set by SD<sub>LVL</sub> and de-asserts low otherwise. SD can be fed back to the enable (EN) input to maintain output stability under a loss-of-signal condition. EN de-asserts the true output signal without removing the input signal. Typically, 4.6dB SD hysteresis is provided to prevent chattering.

This manual provides information on the SY88843V evaluation board. It should be used in conjunction with the SY88843V data sheet, which contains full specifications of the SY88843V.

The SY88843V evaluation board enables fast and thorough evaluation of the SY88843V 3.2Gbps CML low-power limiting post amplifier. The board is an easy-to-use, 4-layer high-speed coplanar design that uses Rogers 4003 dielectric material to achieve high bandwidth. The layer stack is shown in Table 1.

The SY88843V evaluation board is designed to be driven by a high-speed 3.2Gbps pattern generator and is intended to be terminated to a 50Ω scope. The board also provides for simple user adjustability of the SD threshold through the adjustment of an on-board potentiometer. These features allow the user to evaluate various parameters of the SY88843V, as listed in the “Available Measurements” section of this document.

Layer	Definition
1	Signal/GND
2	GND
3	VCC
4	GND

Table 1. SY88843V Evaluation Board Layer Stack-Up

**MEASUREMENT SETUP**

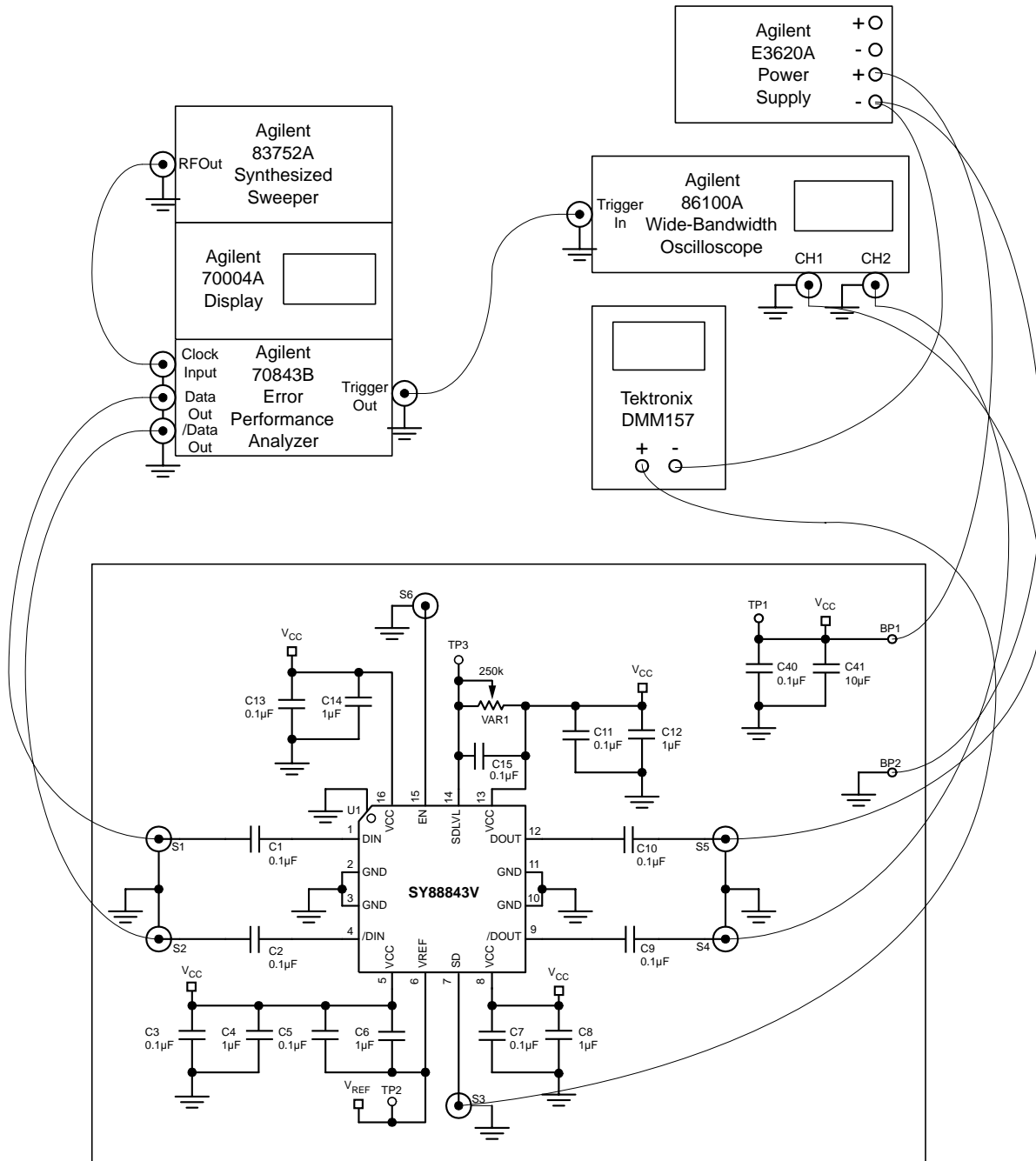
Equipment used for measurements:

1. Agilent 83752A Synthesized Sweeper
2. Agilent 70004A Display
3. Agilent 70843B Error Performance Analyzer
4. Agilent 86100A Wide-Bandwidth Oscilloscope

5. Two (2) MCL BW S15W2 40dB Attenuators
6. Agilent E3620A DC Power Supply
7. Tektronix DMM157 Multimeter
8. Matched High-Speed Cables w/SMA Connectors

**Note:**

Items 1 through 3 constitute the BERT stack.



**Figure 2. Setup for Measurements**

## SETUP FOR MEASUREMENTS

This section explains how to connect and setup the SY88843V evaluation board per Figure 2. Ensure proper ESD precautionary measures are taken before handling sensitive electronic equipment, including the SY88843V evaluation board.

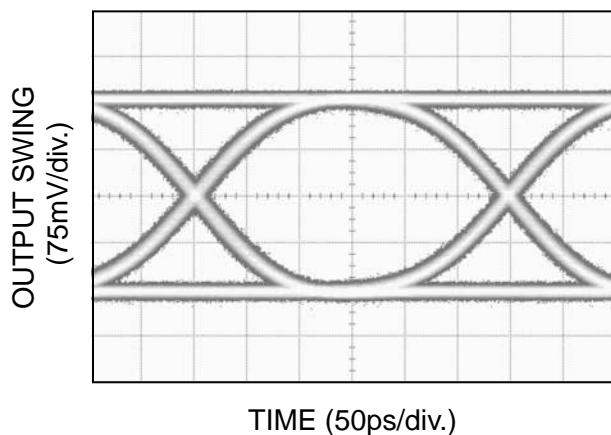
1. Set E3620A output to 3.3V and then turn off E3620A. Connect E3620A's positive lead to  $V_{CC}$  post, negative lead to GND post.
2. Configure Agilent BERT stack:
  - a. Set the 83752A Synthesized Sweeper to 2.5GHz.
  - b. From the 70004A's Pattern menu, choose the PRBS  $2^{31}-1$  pattern.
  - c. From the 70004A's Trigger menu:
    - i. Choose clock as trigger output
    - ii. Choose CLK/8 for divider
  - d. From the 70004A's Data menu:
    - i. External Termination = DC termination 0V
    - ii. Attenuation = 40dB
    - iii. Amplitude = 5mV ( $10mV_{pp}$ )
    - iv. Hi-Level = 0V
    - v. Tracking = ON
    - vi. Polarity = NORMAL
    - vii. Data Output = ON
    - viii. Crossing = 0
3. Connect 70843V's trigger output to 86100A's trigger input.
4. Connect DIN and /DIN (S1 and S2) on SY88843V evaluation board to 70843V's data outputs through 40dB attenuators.
  - a. Connect 40dB attenuators directly to the board rather than the 70843V's data outputs to allow a larger and cleaner signal to pass through the connecting SMA cables.
5. Connect DOUT and /DOUT (S5 and S4) on SY88843V evaluation board to 86100A's inputs.
6. Set DMM157 to display voltage. Connect positive lead to SD (S3) and connect negative lead to GND.
7. Turn on E3620A. Typical power supply current should be ~45mA. Excessive current usually means the power supply leads have been connected backwards. Be careful of this!
8. Configure 86100A oscilloscope
  - a. Verify a trigger signal is present by checking that the Trigger Source button is lit.
    - i. Depress this button to choose external source if necessary
    - ii. Adjust trigger level if necessary
  - b. Press Eye/Mask Mode on front panel.
  - c. Choose NRZ Eye Measurements from on-screen display.
  - d. Choose RMS Jitter, Rise Time, Fall Time and Eye Amplitude Measurements from on-screen selection list.

## MEASUREMENTS

The SY88843V evaluation board assumes the use of a  $50\Omega$  scope to terminate the SY88843V. The following sections detail various measurements that can be performed with the SY88843V evaluation board:

### 1. Eye pattern generation including jitter and rise/fall times:

- Set 70004's Data amplitude to 5mV ( $10\text{mV}_{\text{pp}}$ ).
- Press Autoscale on oscilloscope. The eye pattern should automatically display on the scope. If not, verify the steps listed in the "Setup for Measurements" section are completed. Sometimes the waveform needs to be manually adjusted to fit the display. Use the Time Scale and Voltage Scale knobs on the front panel of the scope to adjust this.
- Observe measurements on scope's display. The rise and fall times should be less than 120ps, amplitude around 400mV ( $800\text{mV}_{\text{pp}}$ ) and jitter around  $10\text{ps}_{\text{rms}}$ .
  - Note that the output amplitude varies with the input amplitude until the SY88843V enters limiting mode at around  $10\text{mV}_{\text{pp}}$  input. The SY88843V has a typical gain of 38dB. Hence,  $5\text{mV}_{\text{pp}}$  input will give only  $400\text{mV}_{\text{pp}}$  output, whereas  $>10\text{mV}_{\text{pp}}$  input will give  $800\text{mV}_{\text{pp}}$  output.



**Figure 3. Typical SY88843V Output Eye Pattern from a  $10\text{mV}_{\text{pp}}$  input at 3.3V, 25°C**

### 2. Mask testing:

- Press Eye/Mask Mode on front panel of scope.
- Choose Mask Testing from on-screen display.
- Choose Open Mask from on-screen selection list.
  - Select and open the OC-48 Mask
- Choose Start Mask Testing from on-screen selection list. Waveform should automatically display with appropriate mask regions and testing will start. If not, verify the steps listed in the "Setup for Measurements" section are completed.

### 3. BER testing:

- Feedback the SY88843V evaluation board's DOUT output to the 70843V's BERT Data input.
- Feedback the 70843V's Clock output to the 70843V's BERT Clock input.
- Set 70004's Data amplitude to 5mV ( $10\text{mV}_{\text{pp}}$ ).
- From the 70004A's Gating menu:
  - Choose a gate condition. The options are: gate by time, errors or bits. Choose bits, but this is of no relevance because there should be no errors, and the test will run forever until manually interrupted if gate by errors is chosen.
  - Choose single gating period
  - Choose run gating
  - 70004A will reset error count and synchronize SY88843V's transmitted bitstream to 70843V's generated bitstream. If synchronization does not occur, it is sometimes due to cable length. Try using different length cables to achieve synchronization. If this is unavailable, another trick is to adjust the 83752A's frequency to a slightly higher or lower value.
  - At end of gating period, there should be no errors

## MEASUREMENTS

### 4. SD hysteresis:

The SY88843V evaluation board provides a potentiometer to allow for easy adjustment of  $SD_{LVL}$  without the need for an extra power supply. The potentiometer acts as a variable resistor which is connected from  $V_{CC}$  to  $SD_{LVL}$ . The SY88843V contains an internal  $2.8k\Omega$  resistor connected from  $SD_{LVL}$  to  $V_{REF}$ .  $V_{REF}$  is a reference voltage of approximately  $V_{CC} - 1.3V$ . Hence,  $SD_{LVL}$  can be set to any voltage from  $V_{CC}$  to  $V_{CC} - 1.3V$ , as specified in the SY88843V data sheet. The potentiometer creates a voltage divider. Thus,

$$SD_{LVL} = V_{CC} - 1.3 \frac{R_{SDLVL}}{R_{SDLVL} + 2.8}$$

where  $R_{SDLVL}$  is the resistance of VAR1 in  $k\Omega$  and voltages are in volts.  $R_{SDLVL}$  is chosen for a desired input sensitivity per the SD assert/de-assert vs.  $R_{SDLVL}$  graph in the SY88843V data sheet. The proceeding steps show how to find the

SD hysteresis for a  $10mV_{pp}$  SD de-assert voltage without measuring  $R_{SDLVL}$ . Other SD de-assert voltages can be used, but the appropriate input signal attenuation is required.

- Set 70004's Data amplitude to  $5mV$  ( $10mV_{pp}$ ).
- Verify DMM157 displays that SD is HIGH ( $\sim 3.3V$ ). If not, turn VAR1 until SD is HIGH.
- Turn VAR1 just until SD is LOW ( $\sim 0.2V$ ).
- Slowly increase 70004A's Data amplitude until SD becomes HIGH. Note the voltage at which SD becomes HIGH. This is the SD assert voltage.
- Now slowly lower the 70004A's Data amplitude until SD becomes LOW again. This should be the starting voltage of  $5mV$  ( $10mV_{pp}$ ). This is the SD de-assert voltage.
- Hysteresis(dB) =  $20\log(\text{SD assert voltage}/\text{SD de-assert voltage})$ . This should be  $\geq 2dB$ .

## FREQUENTLY ASKED QUESTIONS

### **I just got my SY88843V evaluation board and I cannot get anything to work. What should I check first?**

First, check the power supplies. Typical power supply current should be ~45mA. Excessive current usually means the power supply leads have been connected backwards. It is extremely important that the power supply leads are properly connected!

Next, verify that the 70004A's Data outputs are enabled and that there's sufficient amplitude (at least  $10\text{mV}_{\text{pp}}$ ) to drive the SY88843V.

If the above are okay and there's still nothing displaying on the scope, then there's most likely a trigger setup issue with the scope. Look on the scope's front panel and verify that the instrument is triggered. The Trigger Source button should be lit if a trigger signal is present. If not, press the button until the external trigger is selected. Also, try adjusting the level until a signal is found. If this does not work, verify that the 70004A is set to output a CLK/8 trigger signal as described in the "Setup for Measurements" section of this document.

### **Can you suggest a bypass/decoupling scheme?**

Figure 2 shows the power supply decoupling scheme used for the SY88843V evaluation board. The "Bill of Materials" at the end of this document lists the supplier and component values. We have found this arrangement to be an excellent starting point.

### **What layout tips do you have?**

1. Establish controlled impedance stripline, microstrip, or coplanar construction techniques for high-speed signal paths.
2. All differential paths are critical timing paths and skew should be matched to within  $\pm 10\text{ps}$ .
3. Signal trace impedance should not vary more than  $\pm 5\%$ . If in doubt, perform Time Domain Reflectometry (TDR) analysis of signal traces.
4. Place power supply decoupling capacitors as close as possible to the device's power pins.

### **What is Time Domain Reflectometry (TDR)?**

TDR is used to verify impedance continuity along a signal path. Many interconnects, such as SMA, if not launched correctly onto the PCB, will exhibit inductive-like resonance with an abrupt capacitive discontinuity. This discontinuity will subtract signal from the inputs and outputs, effectively closing the resulting data eye. The 86100A allows TDR testing and is a useful tool to help evaluate your PCB.

### **I still have questions. Who should I contact?**

Micrel's HBW Applications hotline is available to assist you. Please call (408) 955-1690 or e-mail [hbwhelp@micrel.com](mailto:hbwhelp@micrel.com) for assistance.

**BILL OF MATERIALS**

Item	Part Number	Manufacturer	Description	Qty
BP1	111-0702-001	Johnson <sup>(1)</sup>	red binding post	1
BP2	111-0703-001	Johnson <sup>(1)</sup>	black binding post	1
C1, C2, C3, C5, C7, C9, C10, C11, C13, C15, C40	PCC1731CT-ND	Panasonic <sup>(2)</sup>	0.1μF surface mount capacitor, size 0402	11
C4, C6, C8, C12, C14, C42	PCC1915CT-ND	Panasonic <sup>(2)</sup>	1μF surface mount capacitor, size 0603	6
C41	PCC1940CT-ND	Panasonic <sup>(2)</sup>	10μF surface mount capacitor, size 1206	1
S1, S2, S4, S5	142-0701-851	Johnson <sup>(1)</sup>	end launch SMA	4
S3, S6	142-0701-201	Johnson <sup>(1)</sup>	PC mount SMA	2
TP1, TP2, TP3	TSW-101-07-S-S	Samtec <sup>(3)</sup>	0.1mil center through hole terminal strip	2
VAR1	3269W-1-254G	Bourns <sup>(4)</sup>	250kΩ potentiometer	1
U1	SY88843V	<b>Micrel, Inc.</b> <sup>(5)</sup>	3.2Gbps CML post amplifier	1

**Notes:**

1. Johnson tel: 800-247-8256
2. Panasonic tel: 800-344-2112
3. Samtec tel: 800-726-8329
4. Bourns tel: 877-426-8767
5. Micrel, Inc. tel: 408-944-0800

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**MICREL, INC. 1849 FORTUNE DRIVE SAN JOSE, CA 95131 USA**

TEL + 1 (408) 944-0800 FAX + 1 (408) 944-0970 WEB <http://www.micrel.com>

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