AN-07

SY89429/30V Frequency Synthesis

Introduction

Micrel's SY89429V and SY89430V frequency synthesizers are designed to be used in various clock subsystems. The primary function of the product is to synthesize clock frequencies required for systems needing a high quality, low jitter clock source.

The cost of other clock sources, either crystal or SAW oscillators, increase dramatically as precision/frequency requirements of digital systems push into the 100+ MHz arena. In the last few years, many low cost CMOS frequency synthesizers have appeared in the market. Unfortunately, these products have relatively high jitter and limited operating frequency range. Therefore, their applications are limited to lower precision/lower frequencies.

The SY89429/30V is designed with Micrel's high-performance ASSET™ Bipolar technology and differential ECL circuit technology throughout. It is a perfect low cost alternative to the expensive crystal or SAW oscillators. Unlike other frequency synthesizers, the SY89429/30V has extremely low jitter and high supply noise rejection that ECL is famous for.

Because the devices are programmable between 25MHz to 950MHz using a 16MHz crystal, different system frequency requirements can all use the same device. This may dramatically reduce inventory costs and management of additional products that are otherwise required to achieve these various frequencies. This programmability also makes board/system speed grading possible as part of the normal production flow without multiple oscillators. This, in turn, provides higher overall yield and lower manufacturing cost.

In addition to cost savings, there are many other benefits to using the SY89429/30V. Normal system production testing can incorporate frequency margining that is unavailable to fixed frequency designs, including crystal or SAW oscillators. This capability leads directly to higher product quality and reliability. Furthermore, the SY89429/30V can be programmed in small steps (1MHz steps with a 16.000MHz crystal). Other precise frequencies can be programmed as well. See sub-section entitled "Advanced Frequency Control Applications." This ability to provide any frequency eliminates the need for the higher cost custom oscillator alternatives.

Throughout this application note, we refer to a frequency range of 25MHz to 950MHz. This is only for simplicity reasons, and makes the application note applicable to both devices.

The VCO range for SY89429V and SY89430V are different. That is, SY89429V has an internal VCO range of 400MHz to 800MHz and an external output frequency of 25MHz to 400MHz. The SY89430V has an internal VCO range of 400MHz to 950MHz and an external output frequency of 50MHz to 950MHz.

General Requirements

Operating the SY89429/30V is very simple. Very few low cost external components are required. These low cost external components provide the tuning capability needed to optimize and minimize jitter characteristics in each individual system application. To achieve the best possible performance in jitter and power supply noise rejection, basic high speed design guidelines should be followed.

Power Supply Requirements

SY89429/30V is designed to operate with a single positive supply of either +3.3V or +5V. The FOUT and /FOUT (the differential PECL outputs) will interface to PECL inputs using the same supply voltage. However, the SY89429/30V can also be used in a true ECL systems. For this application, please refer to the subsection entitled "True ECL Design."

Power Supply Filtering Techniques

As with any high-speed integrated circuits, power supply filtering is very important. A 0.1µF high frequency by-pass capacitor should be used between all separate power supply pins and ground. VCC1, VCC_QUIET, VCC_TTL and VCC_OUT should be individually connected to the power supply plane through vias, and a by-pass capacitor should be used for each pin. To achieve optimum jitter performance, better power supply isolation is required. In this case, a ferrite bead along with a 1µF and a 0.01µF by-pass capacitor should be connected to each power supply pin. Figure 5 shows the connections of the power supply filtering using ferrite beads.

Termination for PECL Outputs

The differential PECL outputs, FOUT and /FOUT, are open emitter outputs. Therefore, terminating resistors or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize waveform distortion. There are a few simple termination schemes. Figure 2 shows three simple termination circuits for a +5V system.

Interface for Inputs

The SY89429/30V is designed to interface with TTL compatible signals. All inputs except XTAL1 and XTAL2 are TTL compatible. These inputs have internal pull up resistors. Therefore, any inputs can be left open–open inputs are logical “1” state. Although inputs can be left open, it is recommended that open inputs be connected to a power supply line. These inputs can be connected to a power supply line (VCC for a logical “1”) or a ground line (VEE for a logical “0”) directly or through series resistors. Alternatively, these inputs can also be driven directly from any TTL-compatible signals. XTAL1 and XTAL2 inputs should only be connected to a crystal.

Input Reference Frequency and On-Chip Crystal Oscillator

The SY89429/30V is designed based on input reference frequency of 16MHz and phase detector frequency of 2MHz. For using other input reference frequencies, refer to subsection entitled “Advanced Frequency Control Applications.” When using a 16MHz reference input frequency, the output frequency can be programmed from 25MHz to 950MHz in 1MHz steps. The input oscillator requires only an off-chip 16MHz reference crystal connected between XTAL1 and XTAL2 pins, and one parallel capacitor. Figure 4a shows the recommended crystal oscillator circuit.

Using the On-Board Crystal Oscillator

The SY89429/30V features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multi-vibrator type design. To reduce sensitivities to loading on the inputs, place the surface mount crystal as close to the SY89429/30V as possible to avoid any board level parasitics. In addition, trace lengths must be matched.

It is recommended that the designer make provisions for a capacitor in parallel with the crystal. A 10pF capacitor should be mounted in parallel with the crystal as this insures crystal start-up (as some crystals may exhibit spurious oscillation frequencies). During power ramp-up, the oscillator transitions from a powered off state to a partially powered up state, and finally to a fully powered up oscillator state. During this transition, the oscillator system can pick up crystal spurious frequencies. This capacitor adds a dominant pole in the system and prevents these unwanted oscillations. This 10pF capacitor will lower oscillating frequency by about 250ppm.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Table 1 specifies the performance requirements of the crystals to be used with the SY89429/30V.

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150ppm 0°C to 70°C
Operating Range	0°C to 70°C
Shunt Capacitance	5pF to 7pF
Equivalent Series Resistance (ESR)	50Ω to 80Ω
Correlation Drive Level	100µW
Aging	5ppm/Yr (First 3 years)

Table 1. Crystal Specifications

Filter Design

The filter for any Phase Locked Loop (PLL) based device deserves special attention. The SY89429/30V provides filter pins for an external filter. A simple three-component passive filter is recommended for achieving ultra low jitter. Figure 4b shows the recommended three-components. Due to the differential design, the filter is connected between LOOP_FILTER and LOOP_REF pins. With this configuration, extremely high supply noise rejection is achieved. It is important that the filter circuit and filter pins be isolated from any non-common mode coupling and placed in the VCC plane.

Generating High-Speed TTL Clock Signals

A high speed PECL-to-TTL translator such as SY10/100ELT23 or SY10/100ELT23L (for +3.3V) may be used to generate high speed TTL compatible signals. High speed PECL-to-TTL translating Clock Drivers such as the SY10/100H841/842 or the SY10/100H641/646 may be added if multiple copies of such clocks are desired. For a 3.3V power supply operation, the following PECL-to-TTL translating clock drivers, the SY10/100H841L/842L, or the SY10/100H641L/646L may be used. These translators are capable of driving 50pF loads up to 160MHz.

True ECL Design

The SY89429/30V is designed for TTL/PECL systems. However, it can be easily designed into a pure ECL environment. Connect all VCC pins to ground and all GND pins to -3.3V, -4.5V (or -5.2V) power supply line. With this operating condition, FOUT and /FOUT interface directly with normal 100K ECL signals. All other inputs have internal pull up resistors. Therefore, any input can be left open and open inputs are logical “1” state. Although inputs are allowed to be open, it is recommended that open inputs be connected to a power supply line. These inputs can be connected to ground lines (0 volt for a logical “1”) or negative power supply lines (-3.3V, -4.5V or -5.2V for a logical “0”) directly or through series resistors. These inputs can interface to normal ECL signals with the SY100ELT23 for signal translation. Figure 1 shows the schematic with signal translations.

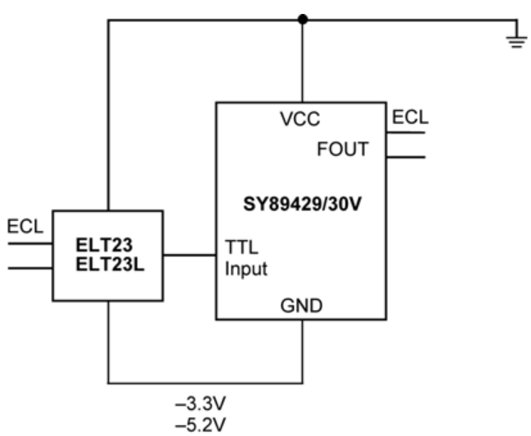

Figure 1. Interfacing to SY89429/30V TTL Inputs with ECL Signals for True ECL Designs

Advanced Frequency Control Applications

The primary function of these products is to synthesize clock frequencies from 25MHz to 950MHz in 1MHz steps with a 16.00MHz crystal. However, there are many other applications that are not so obvious. Even though the SY89429/30V is said to be able to generate frequencies between 25MHz to 950MHz, in 1MHz steps with a 16MHz crystal, output frequency is programmed by properly configuring the internal dividers and can be represented by this formula:

$$FOUT = \frac{FXTAL}{8} \times \frac{M}{N}$$

$$Step\ Size = \frac{FXTAL}{8} \times \frac{1}{N}$$

$$FVCO = \frac{FXTAL}{8} \times M$$

Where

FXTAL is the crystal frequency or input reference frequency

M is the VCO frequency multiplier (from 128 to 511)

N is the post divider (1, 2, 4, 8, or 16)

FVCO is the VCO frequency (400MHz to 950MHz)

Crystal oscillator frequency is designed to be less than 25MHz using a fundamental crystal. Input frequencies at the low end are limited to above 6.26MHz due to minimum VCO frequency of 400MHz.

Using the FOUT equation, it is very easy to determine what M and N values must be for a certain multiplication factor.

Application Examples

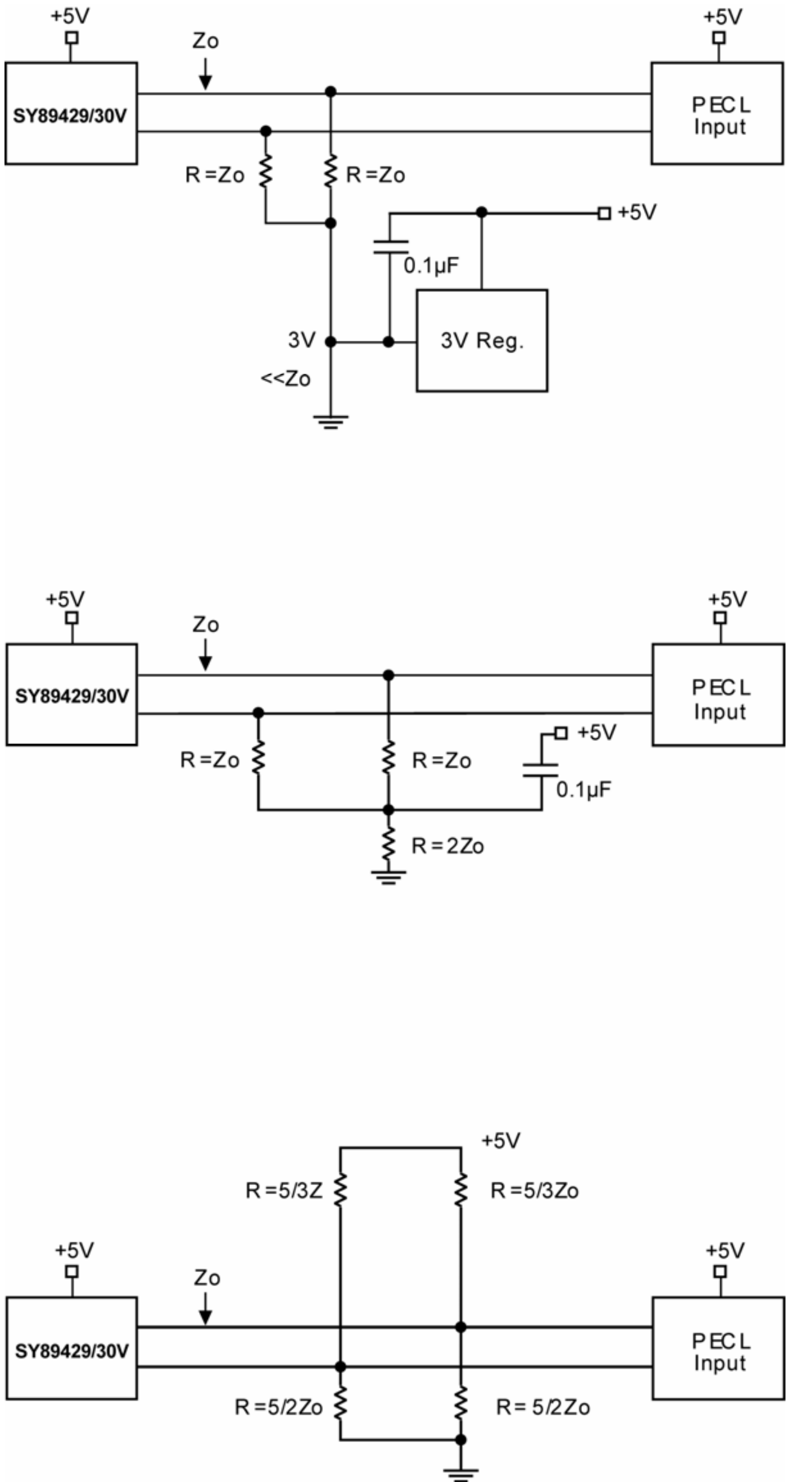

Figure 2. Matched Impedance Termination Schemes for 5V Systems

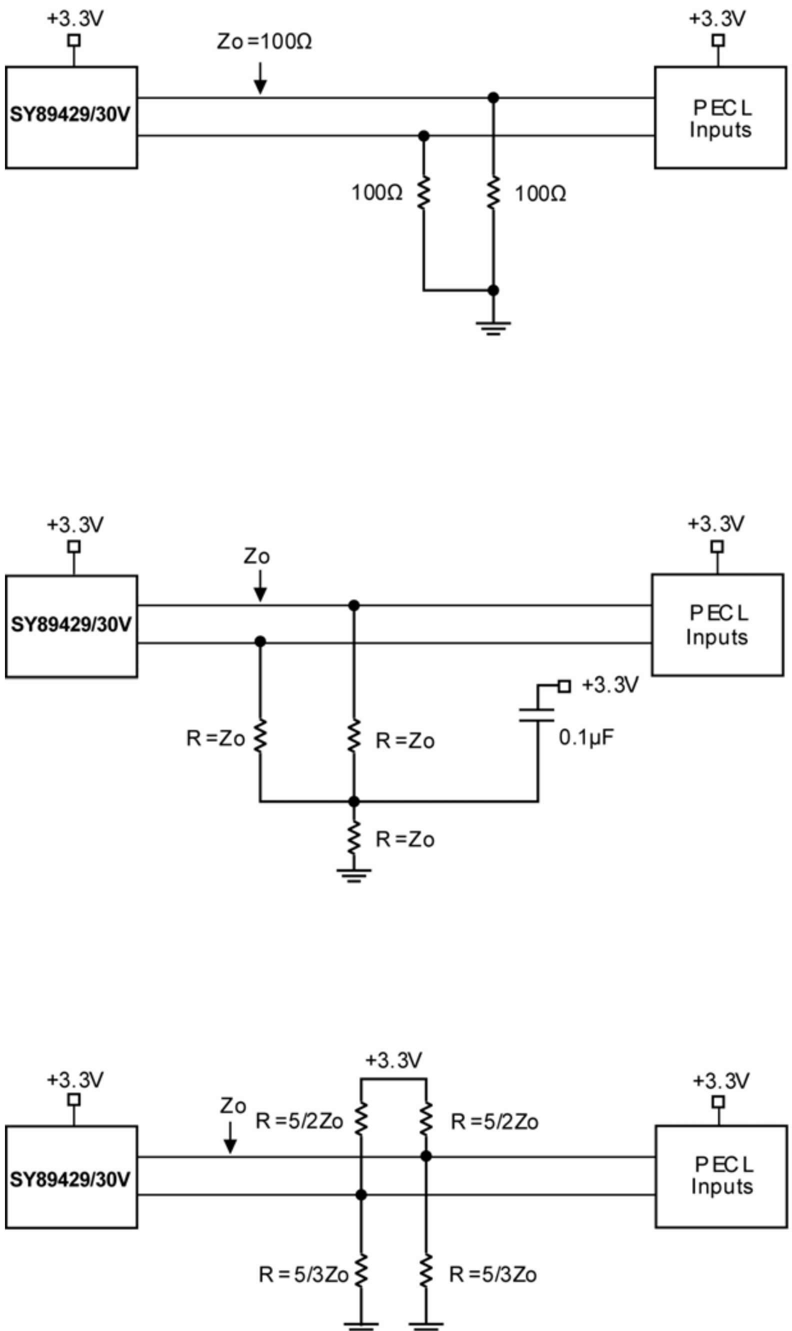

Figure 3. Matched Impedance Termination Schemes for 3.3V Systems

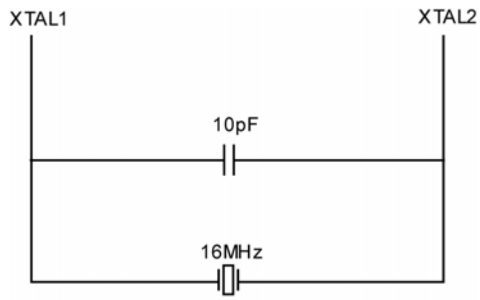

Figure 4a. Recommended External Components for Crystal Oscillator

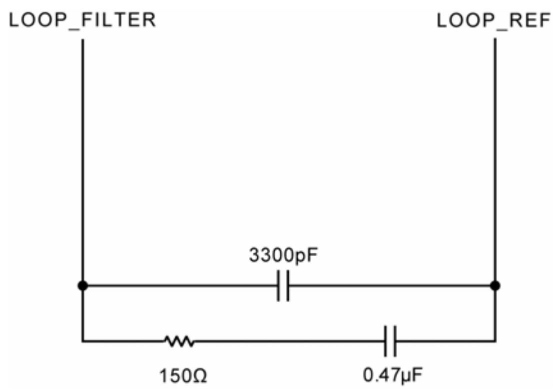

Figure 4b. Recommended Passive Filter Circuit

hbwhelp@micrel.com or (408) 955-1690

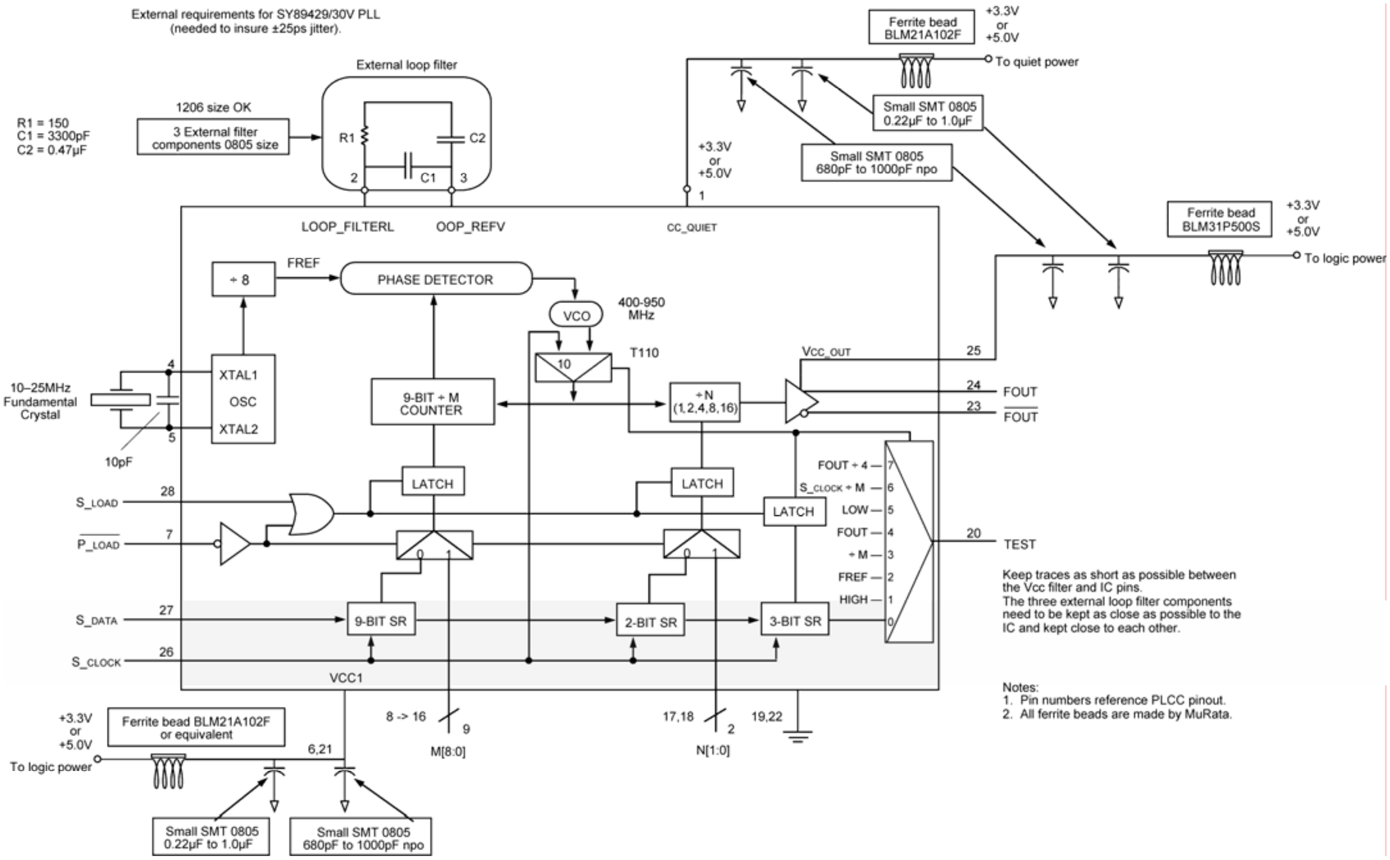

Figure 5. Power Supply Filtering

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com